Embedded System Design for Wireless Applications

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DAC 2000, Los Angeles

The Distributed Approach to Information Processing

The "last meter" problem to information access

Source: Richard Newton
The Smart Home

Dense network of sensor and monitor nodes

Security
Environment monitoring and control
Object tagging
Identification

Wireless in the Home

Home-networked households in the United States, in thousands

Source: IEEE Spectrum, December 99
The Changing Metrics

Performance as a Functionality Constraint
(“Just-in-Time Computing”)

The Wireless System Design Challenge

The Battery Limitation

- Projected energy per digital operation (2004): 50 pJ
- Lithium-Ion: 220 Watt-hours/kg == 800 Joules/gr
- At 50 pJ/operation: 10 teraOps/gr!
  - Equivalent to continuous operation at 100 MOPS for 30 hours (or average power dissipation of 6 mW)
Some interesting numbers

- **Energy cost of digital computation**
  - 1999 (0.25µm): 1pJ/op (custom) … 1nJ/op (µproc)
  - 2004 (0.1µm): 0.1pJ/op (custom) … 100pJ/op (µproc)
    • Factor 1.6 per year; Factor 10 over 5 years
    • Assuming reconfigurable implementation: 1 pJ/op

- **Energy cost of communication**
  - 1999 Bluetooth (2.4 GHz band, 10m distance)
    • 1 nJ/bit transmission energy (thermal limit 30 pJ/bit)
    • Overall energy: 170 nJ/bit reception / 150 nJ/bit transmission (!)
    • Standby power: 300 µW
  - 2004 Radio (10 m)
    • Only minor reduction in transmission energy
    • Reduce transceiver energy with at least a factor 10-50

- **Trade-off**
  - @10m: 5000 operations / transmitted bit
  - @ 1m: 0.5 operations / transmitted bit

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The Implementation Opportunities

**System-on-a-Chip**

- Multi-Spectral Imager
- 500 k Gates FPGA + 1 Gbit DRAM
- Preprocessing
- Analog
- 64 SIMD Processor Array + SRAM
- Image Conditioning
- 100 GOPS
- µC system +2 Gbit DRAM Recognition

Embedded applications where cost, performance, and energy are the real issues!
DSP and control intensive
Mixed-mode
Combines programmable and application-specific modules

SOC anno 2010
The System-on-a-Chip Nightmare

“Femme se coiffant”
Pablo Ruiz Picasso
1940

The “Board-on-a-Chip” Approach

Courtesy of Sonics, Inc
The Wireless Challenge

The Software Radio

- Idea: Digitize (wideband) signal at antenna and use signal processing to extract desired signal
- Leverages of advances in technology, circuit design, and signal processing
- Software solution enables flexibility and adaptivity, but at huge price in power and cost
- 16 bit A/D converter at 2.2 GHz dissipates 1 to 10 W
The Mostly Digital Radio

The Mostly Digital Radio

Analog

Digital

RF input ($f_c = 2$GHz)

LNA

chip boundary

$\cos[2\pi(2\text{GHz})t]$

$\sin[2\pi(2\text{GHz})t]$

Digital Baseband Receiver

I (50MS/s)

Q (50MS/s)

Analog Digital

Architectural Choices

Flexibility

1/Efficiency

Dedicated Logic

Direct Mapped Hardware

Hardware Reconfigurable Processor

Satellite Processor

Satellite Processor

Software Programmable DSP

MAC Unit

Addr Gen

Prog Mem

$\mu$P

Prog Mem

$\mu$P

General Purpose $\mu$P
The Energy-Flexibility Gap

![Energy-Flexibility Gap Diagram](image_url)

System Optimization Hierarchy

![System Optimization Hierarchy Diagram](image_url)
The fully programmable approach

- Flexible platform for experimentation on networking and protocol strategies
- Size: 3”x4”x2”
- Power dissipation < 2 W (peak)
- Multiple radio modules: Bluetooth, Proxim, …
- Collection of sensor and monitor cards
- Fully operational by late spring (including software support system)!

Digital Intercom — A Design Exercise in Communication/Component Based Design

- Known and tested specification of limited complexity allows focus on architectural implementation methodology
- Two-chip implementation leverages separates between analog (RF) and digital design concerns
- Duration of exercise: 1 year (summer ‘00)

Up to 20 users per cell @ 64 kbit/sec per link
TDMA selected as MAC protocol
Two-Chip Intercom

Direct down-conversion front-end
(Yee et al)

The Target Architecture

Multi-model Analog RF

Fixed Hardware

Physical Layer

Accelerators (bit level)

Timing recovery

Embedded µP

Appl.
Keypad Display
Coding
ARQ

Correlators
MUD
Filters
MAC Transport

Programmable Hardware
Digital Baseband

Stage 1: floating point blocks
Stage 2: fixed point blocks

Design Estimations (First order):

RF + ADC/DAC
  Transmit: 30 mW
  Receive: 70 mW

Digital (conservative)
  Transmit: 20 mW (100,000 transistors)
  Receive: 80 mW (700,000 transistors)

Physical layer timing analysis (from Simulink)

Abstracted Simulation Results Drive Protocol Design!

Estimates for the performance of the TCI Physical layer

<table>
<thead>
<tr>
<th>Rate</th>
<th>Duration</th>
<th>Additional Calculations</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MHz</td>
<td>s</td>
<td></td>
</tr>
<tr>
<td>Chip</td>
<td>2.50E+07</td>
<td>25.00 4.00E-08 0.04</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>8.06E+05</td>
<td>0.81 1.24E-06 1.24</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit</td>
<td>1.61E+06</td>
<td>1.61 6.20E-07 0.62</td>
</tr>
<tr>
<td>Pilot symbol</td>
<td>1.24E-06</td>
<td>1.24</td>
</tr>
<tr>
<td>Pilot sequence length</td>
<td>1.86E-05</td>
<td>1.86</td>
</tr>
<tr>
<td>Pilot sequence</td>
<td>1.90E-05</td>
<td>1.90</td>
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<tr>
<td></td>
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</tr>
</tbody>
</table>

The selected protocol will send a pilot sequence, a small number of dummy data bits (PD), another pilot sequence, and the real data bits (DAT) with the constraint that DAT < safe # sequential symbols

|                |                |                |
|                |                |                |

The time from RX to TX transition until:
- First DAT clock on transmitter
- Last DAT clock on transmitter
- Radio turn-around

The time from TX on radio A until:
- RECV on radio B
- DAT2 RECV on radio B

The time from TX on radio A, and RX on radio B until:
- DAT2 RECV on radio B

Tool: Microsoft Excel

Radio Turn-around Time

Abstracted Simulation Results Drive Protocol Design!
Physical Layer Design

Digital baseband bridges gap between RF/Comm and protocol/network

Physical to Protocol Interface

- Different tools
- Verification relying on co-simulation
- Interface design critical to ensuring final designs work together
  - Define small number of interface signals
  - Clearly specify behavior
The Intercom Protocol Stack

- User Interface Layer
  - UI

- Transport Layer
  - Transport

- Mac Layer
  - Filter
  - MAC

- Data Link Layer
  - Transmit
  - Receive
  - Synchronization
  - Tx_data
  - Tx/Rx
  - Rx_data

Refinement-based Protocol Design Methodology

A CFSM-based approach

Advantages
- Combines synchronous and asynchronous models
- Constrained model enables verification
Co-design Finite State machines

- Three-level hierarchy
  - top level: asynchronous, partially ordered
    (bounded buffer non-blocking single-read communication)
  - middle level: synchronous FSM
    (atomic event- and condition-based transition)
  - bottom level: Synchronous DataFlow-like
    (FSM provides tokens and selects active sub-network)

(from ee249: http://www-cad.eecs.berkeley.edu/Respep/Research/hsc/class/index.html)
**POLIS/VCC Design Flow**

* (from the VCC manual)

**Describing the Behavior**

<table>
<thead>
<tr>
<th>Layer</th>
<th>C-code (lines)</th>
<th>State-transition Diagram (states)</th>
</tr>
</thead>
<tbody>
<tr>
<td>User Interface</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Modem</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Transport</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>MAC</td>
<td>270</td>
<td>42</td>
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<tr>
<td>Transmitter</td>
<td>120</td>
<td>16</td>
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<tr>
<td>Receiver</td>
<td>140</td>
<td>2</td>
</tr>
<tr>
<td>Synchronization</td>
<td></td>
<td>17</td>
</tr>
</tbody>
</table>

- GFSM
- VCC, Polis
Formal Verification

• **System satisfies certain properties?**
  – System described in some formal mathematical languages (e.g. Esterel)
  – Properties written in some formal logic (e.g. LTL) or formal model (e.g. Esterel)

• **Property Verification**
  – Invariant (only one remote can send voice data in any time slot)
  – Response (if a remote sends a request to the base station, then eventually there is an acknowledgement)
  – deadlock freedom

• **Refinement Checking**
  – Does the (low-level) implementation conform with the (high-level) specification?
    (Do the mapped CFSMs function the same as the specification?)

• **Mocha (Henzinger): Modularity in Model Checking**

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Example of Property Verification

Remote returns to the **disconnect state** if user presses the **disconnect button**.

\[ AG(\text{Disc} \rightarrow \text{AF(Not Conn)}) \]

**NOT OK**
Why it Fails?

- Remote accepts Disc from the user even if it is not connected
- After the remote has sent DiscReq and waits for acknowledgement
- However, base station ignores DiscReq if remote is not registered

Targeted Implementation Platform

Embedded Processor

Memory Sub-system

Interconnect Network

Baseband Processing

Configurable Logic (Physical Layer)

Programmable Protocol Stack

Benefit: Build library of computational and networking modules (and models)
Describing the Architecture

- **Xtensa embedded CPU (Tensilica, Inc)**
  - Configurability allows designer to keep “minimal” hardware overhead
  - ISA (compatible with 32 bit RISC) can be extended for software optimizations
  - Fully synthesizable
  - Complete HW/SW suite
- **VCC modeling for exploration**
  - Requires mapping of “fuzzy” instructions of VCC processor model to real ISA
  - Requires multiple models depending on memory configuration
  - ISS simulation to validate accuracy of model

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Describing The Architecture

The On-Chip Network

Example: “The Silicon Backplane” (Sonics, Inc)
Describing the Architecture

- SONICS model in VCC

- Flexible bandwidth arbitration model
  - TDMA slot map gives slot owner right of refusal
  - Unowned/unused slots fall to round-robin arbitration
  - Latency after slice granted is user-specified between 2-7 Bus Clock cycles

TCI Architecture

- ASIC
- SiliconBackplane
- Tensilica Xtensa
Exploring Architectural Mappings

Software Processor
Application
Transport
Mu-law
MAC
ASIC
Accelerators
Rest

Processor Utilization - Estimation

Processor Utilization
32.7%
2.7%
5.46%

Transport User Interface
ARM @1MHz

Mulaw Transport User Interface
ARM @11MHz

0.5 MAC Mulaw Transport User Interface
ARM @200MHz

0.9 MAC Mulaw Transport User Interface
ARM @2GHz

Latency insensitive
Peak performance
RTOS overhead
Clock Frequency
**Implementation Fabrics for Protocols**

A protocol = Extended FSM

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**Intercom TDMA MAC**

**Implementation alternatives**

<table>
<thead>
<tr>
<th></th>
<th>ASIC</th>
<th>FPGA</th>
<th>ARM8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>0.26mW</td>
<td>2.1mW</td>
<td>114mW</td>
</tr>
</tbody>
</table>

ASIC: 1V, 0.25 μm CMOS process
FPGA: 1.5V 0.25 μm CMOS low-energy FPGA
ARM8: 1V 25 MHz processor; n = 13,000
Ratio: 1 - 8 - >> 400

Idea: Exploit model of computation: concurrent finite state machines, communicating through message passing
HW Mapping Experiment: STD to Std. Cell

Area Comparison – Manual versus Automated

HW Mapping Experiment: STD to FPGA

Area Comparison – Manual versus Automated
**HW Mapping Experiment: Power**

**FPGA versus PLD**

![Bar chart comparing Power Consumption between FPGA and PLD](chart.png)

**Hierarchy in System Optimization**

*Network level*
- Functional & Performance Requirements
- Performance analysis
- Node Architecture

*Node level*
- Functional & Performance Requirements
- Node Architecture
- Performance analysis

*Constraints*
The Applications and Specs

The Obvious Choice - The Smart Home and Network Appliances

Dense network of sensor and monitor nodes

Security
Environment monitoring and control
Object tagging
Identification

System Requirements and Constraints

- Large numbers of nodes — between 0.05 and 1 nodes/m²
- Cheap (<0.5$) and small (< 1 cm³)
- Limited operation range of network — maximum 50-100 m
- Low data rates per node — 1-10 bits/sec average
  - up to 10 kbit/sec in rare local connections to potentially support non-latency critical voice channel
- Crucial Design Parameter:
  Spatial capacity (or density) — 100-200 bits/sec/m²
The Software-Defined Radio

System-Level Design Space Exploration

Implementation in hard- and software

• Based on well-defined abstraction layers
• Step-wise refinement (partitioning, resource mapping and sharing) enables correctness verification
• Automatic synthesis of adaptive protocols in hard- and software
**PicoRadio Energy Optimization**

*The Cost of Communication*

Assumes $R^4$ loss due to ground wave (@ 1 GHz)

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**Transmit Power**

-70dBm
-30dBm
10dBm
90dBm

**Distance**

1m 10m 100m 1Km 10Km

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**Communicating over Long Distances**

*Multi-hop Networks*

Example:
- 1 hop over 50 m
  1.25 nJ/bit
- 5 hops of 10 m each
  $5 \times 2 \text{ pJ/bit} = 10 \text{ pJ/bit}$
- Multi-hop reduces transmission energy by 125!
  (assuming path loss exponent of 4)

But … network discovery and maintenance overhead
Comparing the approaches from an energy perspective

- Energy = Eb * Packet Size
- Reactive Routing good for rarely used routes
- Proactive Routing good for frequently used routes
- Need solution that is more adequate for problem at hand: class-based and location-based addressing.
Summary

• Low-energy design ascends to prime time forced mainly by the last-meter problem
• System-on-a-Chip approach enables and demands heterogeneous implementation strategies, sometimes involving non-intuitive and innovative design platforms
• Design exploration over various fabrics and partitions has dramatic impact on dominant metrics, such as energy and cost
• It requires orthogonalization of function and architecture, supplemented with performance models (cost, time, energy)
• This methodology holds at all levels of the system hierarchy