EE290C - Spring 2004
Advanced Topics in Circuit Design
High-Speed Electrical Interfaces

Lecture #26
Case Studies:
  XAUI, PCI-Express
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4/22/04

Agenda

» Project phase-II discussion
» Case studies
  » XAUI
  » PCI Express
Project Phase-II

- Assignments clear?
- Impact from circuits yet?
- Significant issues?

XAUI

- XAUI = 10G Attachment Unit Interface
- Origins in 10G Ethernet 802.3ae
  - Extended into backplane space
- Defines device characteristics
  - BUT
    - Also defines loss characteristics & system parameters
    - Also budgets system voltage & timing
    - A lot of the terminology used has become common; a mixture from different backgrounds, i.e. SONET, etc.
Where XAUI Fits

- Clearly an extension, but one of the first good definitions of a serial link architecture & requirements

XAUI Architecture – Basic Qualities

- Bundle of 4 pairs @ 2.5Gb/s/pair (delivered) = 10Gb/s
- 8b10b coding => raw line rates are 3.125Gb/s
- AC coupled for interoperability (at receiver)
- 100Ω differential
- Can practically achieve eyes with 1 or 2 tap TXeq
- Plesiochronous between quads; +/- 100ppm in system
- Lane deskewing handled at an upper layer (XGXS)
- BER is defined as < 10^{-12}
- Spec includes methods for testing compliance (!)
XAUI Driver Characteristics

![Diagram of XAUI Driver Characteristics]

Figure 47-3—Driver output voltage limits and definitions

- $[L_i^{P_T}]$ and $[N_i^{L_T}]$ are the positive and negative sides of the differential signal pair for Lane $i$ ($i = 0, 1, 2, 3$)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Built-in reference</td>
<td>3.125 GHz ± 100 ppm</td>
<td>OBO ppm</td>
</tr>
<tr>
<td>Unit interval nominal</td>
<td>128 pc</td>
<td></td>
</tr>
<tr>
<td>Differential amplitude minimum</td>
<td>1800 $V_{PE}$</td>
<td></td>
</tr>
<tr>
<td>Absolute output voltage limits</td>
<td>2.5 V</td>
<td></td>
</tr>
<tr>
<td>Differential output return loss minimum</td>
<td>[See Figure (17-4)]</td>
<td>dB</td>
</tr>
</tbody>
</table>

Output jitter
- Near-end maximum:
  - $± 0.175$ peak-to-peak from the mean
  - $± 0.257$ peak-to-peak from the mean
  - $± 0.290$ peak-to-peak from the mean
  - $± 0.275$ peak-to-peak from the mean

- Far-end maximum:
  - $± 0.175$ peak-to-peak from the mean
  - $± 0.257$ peak-to-peak from the mean

- Total jitter:
  - $± 0.290$ peak-to-peak from the mean

- Differential jitter:
  - $± 0.275$ peak-to-peak from the mean

$\gamma_1 = -40$ dB for 32.5 MHz < $F_{eq}$ < 625 MHz, and
$-10 + 10 \log (625)$ dB for 625 MHz < $F_{eq}$ < 3.125 GHz

XAUI Driver Template

![Diagram of XAUI Driver Template]

Figure 47-4—Driver template

- Specified at both Tx & Rx ends (implied channel)
- Accounts for both attenuation and uncompensated ISI

Table 47-2—Driver template intervals

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Near-end value</th>
<th>Far-end value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>0.275</td>
<td>0.275</td>
<td>UI</td>
</tr>
<tr>
<td>X2</td>
<td>0.360</td>
<td>0.400</td>
<td>UI</td>
</tr>
<tr>
<td>A1</td>
<td>400</td>
<td>100</td>
<td>$nV$</td>
</tr>
<tr>
<td>A2</td>
<td>800</td>
<td>800</td>
<td>$nV$</td>
</tr>
</tbody>
</table>
**XAUI Receiver Characteristics**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band rate tolerance</td>
<td>3.125 ± 0.000</td>
<td>GBd</td>
</tr>
<tr>
<td>Unit interval (UI) nominal</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>Receiver coupling</td>
<td></td>
<td>AC</td>
</tr>
<tr>
<td>Return loss* differential common mode</td>
<td>10 6 0</td>
<td>dB dB</td>
</tr>
<tr>
<td>Jitter amplitude tolerance</td>
<td>0.65</td>
<td>UI&lt;sub&gt;p-p&lt;/sub&gt;</td>
</tr>
</tbody>
</table>

*Relative to 100 Ω differential and 25 Ω common mode. See 47.3.4.5 for input impedance details.

**XAUI Jitter Tolerance**

- **Jitter separated into 3 pieces**
  - DJ: Deterministic jitter (includes residual ISI, duty-cycle error, etc.)
  - RJ: Random jitter – uncorrelated with any source
  - SJ: Sinusoidal jitter
    - Doesn’t necessarily exist in a real system, but used in tolerance as a way of making sure system can track low frequency wander, Vdd effects

- **XAUI jitter tolerance specs**
  - Receiver must be able to tolerate this much jitter
  - DJ: 0.37 UI<sub>p-p</sub>
  - DJ+RJ: 0.55 UI<sub>p-p</sub>
  - SJ: additional SJ (on top of DJ+RJ) to limit of mask…
**XAUI Jitter Tolerance: SJ Mask**

![Graph showing sinusoidal jitter amplitude over frequency]

**XAUI Example System Budgeting**

- Supposed to represent a system with 50cm of FR4
- Sound familiar?

<table>
<thead>
<tr>
<th></th>
<th>Loss (dB)¹</th>
<th>Differential skew (ps-p-p)</th>
<th>Total jitter (UL_{p-p})²</th>
<th>Deterministic jitter (UL_{p-p})²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driver</td>
<td>0</td>
<td>15</td>
<td>0.35</td>
<td>0.17</td>
</tr>
<tr>
<td>Interconnect</td>
<td>7.5</td>
<td>60</td>
<td>0.20</td>
<td>0.20</td>
</tr>
<tr>
<td>Other</td>
<td>4.5</td>
<td></td>
<td>0.10</td>
<td>0.10</td>
</tr>
<tr>
<td>Total</td>
<td>12.0</td>
<td>75</td>
<td>0.65</td>
<td>0.47</td>
</tr>
</tbody>
</table>

¹Budgetary loss in height of eye opening.
²Includes such effects as crosstalk, noise, and interaction between jitter and eye height.
³Jitter specifications include all but 10⁻¹² of the jitter population.
Example XAUI Implementation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Experimental Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driving range</td>
<td>1.0 - 3.3 V</td>
</tr>
<tr>
<td>Input sensitivity at 100 MHz</td>
<td>200 mV differential</td>
</tr>
<tr>
<td>Transmitter data rate (MIN)</td>
<td>650 Mbps (max)</td>
</tr>
<tr>
<td>Transmitter data rate (MAX)</td>
<td>1.2 Gbps</td>
</tr>
<tr>
<td>Minimum receive input sensitivity</td>
<td>60 mV</td>
</tr>
<tr>
<td>Maximum receive input sensitivity</td>
<td>100 mV</td>
</tr>
<tr>
<td>Power supply</td>
<td>1.5 V, 1.8 V</td>
</tr>
<tr>
<td>Transmitter power dissipation</td>
<td>100 mW</td>
</tr>
</tbody>
</table>

Wadhwa, CICC 2003, 0.13µ CMOS

Agenda

- Project phase-II discussion
- Case studies
  - XAUI
  - PCI Express
History: PCI Bus Factoids

- PCI = Peripheral Component Interconnect
- Original PCI Bus standardized in 1992
- Characteristics
  - 32-bits @ 33 MHz (BW = 133MB/sec)
  - Single-ended, Synch., Multi-drop parallel bus
  - Requires clock/data trace matching
- Evolved to several variations:
  - PCI-X, CompactPCI, etc.

Synchronous Busses Need Trace Matching

- At high speed, timing skews are a major issue
- Serpentines on PCB needed to address this
- May be OK upto 1 Gbps
Bus Evolution

PCI Express: Based on Serial Links

- Characteristics
  - 1x, 2x,..., 32x @2.5 Gbps (BW = up to 8 GB/sec)
  - Point-to-point differential signaling
  - No separate clock signal (embedded clks)
  - Link-end RefCks can be independent
  - No trace matching required between lanes

- Benefits
  - Bandwidth scalability
  - Higher line speeds
  - Lower cost
  - Higher speed & manufacturable
PCI Express: Where it fits

- **Bandwidth Scalability**
  - Cheaper connectors & smaller board areas
  - Next gen PCI Express expected to support 5-6.25Gbps

- **Legacy support w/ PCI**
  - Software/driver level

- **Advanced capabilities**
  - Ease-of-use (plug&play)
  - Power management
  - Features for communications systems

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PCI Express – Basic Qualities

- **Similar**
  - 8b10b coding => raw line is 2.5Gb/s; delivered is 2G
  - AC coupled for interoperability (at transmitter)
  - 100Ω differential

- **Different**
  - Unit is a single TX/RX differential pair @ 2.5Gb/s/pair
    - Support for x1, x2, x4, x8 in specifications
    - Plesiochronous at +/- 300ppm
    - Support for spread-spectrum-clocking
    - Gen-II plan for performance scaling to 6G
    - Becon detect, power states to allow lower off current
    - Built-in requirement for de-emphasis (TxEq)
    - Lane deskewing handled at an upper layer (XGXS)
The Packet Paradigm Pushing Into PCs

> Trigger events routinely require sequencing across multiple events and busses

"Read" & "Write" Cycles replaced by Packets

![Diagram of packet paradigm]

Request Header Format
For 64-bit addressing of memory

Completion Header Format

Courtesy Agilent
### PCI Express: Transmitter Specification

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>UI</td>
<td>Unit Interval</td>
<td>399.88</td>
<td>400</td>
<td>400.12</td>
<td>ps</td>
<td>Each UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations. See Note 1.</td>
</tr>
<tr>
<td>$V_{TX-DIFF-P}$</td>
<td>Differential Peak to Peak Output Voltage</td>
<td>0.800</td>
<td>1.2</td>
<td></td>
<td>V</td>
<td>$V_{TX-DIFF-P} = 2*V_{TX-DL} - V_{TX-CL}$ See Note 2.</td>
</tr>
<tr>
<td>$V_{TX-DE-RATIO}$</td>
<td>De-Emphasized Differential Output Voltage (Ratio)</td>
<td>-3.0</td>
<td>-3.5</td>
<td>-4.0</td>
<td>dB</td>
<td>This is the ratio of the $V_{TX-DIFF-P}$ of the second and following bits after a transition divided by the $V_{TX-DIFF-P}$ of the first bit after a transition. See Note 2.</td>
</tr>
<tr>
<td>$T_{TX-EYE}$</td>
<td>Minimum TX Eye Width</td>
<td>0.70</td>
<td></td>
<td></td>
<td>UI</td>
<td>The maximum Transmitter jitter can be derived as $T_{JITTER} = 1 - T_{TX-EYE}$. See Notes 2 and 3.</td>
</tr>
</tbody>
</table>

### PCI Express: Transmitter Equalization

- Simple single-tap equalizer defined as de-emphasis for subsequent identical bits (CIDs)
- Defined as driven at 3.5dB below first bit
PCI Express: Everything else about the TX too!

- Many other specs involving idle, tRF, etc.
- A more complete spec needed for true multi-vendor compatibility
  - But basic performance requirements not all that different from XAUI

TX Compliance

- Not that new... but TxEq is well defined
  - Note also: bits no longer have flat spots!
PCI Express: Receiver Specification

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Norm</th>
<th>Max</th>
<th>Units</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Unit Interval</td>
<td>395.88</td>
<td>400</td>
<td>400.12</td>
<td>ps</td>
<td>The UI is 400 ps ± 300 ps. UI varies ± 0.7 ns, depending on the measurement equipment.</td>
</tr>
<tr>
<td></td>
<td>Differential Input Peak to Peak Voltage</td>
<td>0.175</td>
<td>1.22</td>
<td>6</td>
<td>V</td>
<td>(V_{	ext{MAXIMUM}} = 2V_{	ext{MIN}} ) \ (V_{	ext{MINIMUM}} ) Section 7.</td>
</tr>
<tr>
<td></td>
<td>Minimum Receiver Eye Width</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
<td>UI</td>
<td>The receiver eye width is defined as the instantaneous deviation of the measured waveform from the median. The receiver eye width is measured at the center of the clock transition, as defined in Section 6.2.2.</td>
</tr>
<tr>
<td></td>
<td>Maximum time between bit errors</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>UI</td>
<td>The maximum time between bit errors is defined as the maximum time between bit errors. As defined in Section 6.2.2.</td>
</tr>
<tr>
<td></td>
<td>AC Peak Crowbar Mode Input Voltage</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>mV</td>
<td>(V_{	ext{MAXIMUM}} = 2V_{	ext{MINIMUM}} ) (V_{	ext{MINIMUM}} = 0.05 ) (V_{	ext{MINIMUM}} ) Section 12.</td>
</tr>
<tr>
<td></td>
<td>Differential Return Loss</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>dB</td>
<td>Measured under 0 MHz to 1.25 GHz within 0 dB and 0.75 dB bandwidths, 0.05 mV, and 0.05 mV, respectively. Section 9.</td>
</tr>
</tbody>
</table>

RX Compliance

- Input is now 175mV (p-p diff) x 0.4UI
- TX Transition bit is 800mV x 0.7UI
- TX De-emphasis bit is 566mV x 0.7UI
- Q: What does this mean viz. loss at Nyquist?
Additional Features for PCI Express PHY

- New Features required for Hot-Plug capability, Power Mgmt
  - Transmitter Tri-state (‘Electrical Idle’) Capability
  - Receiver termination is to ground instead of Vdd
  - ‘Rx Detect’ feature before transmission
  - Beacon Generate/Detect Feature for Remote System Wakeup
  - Exhaustive Power Management features

Tx-Idle & Receiver Detect Feature

- To support Hot plug
  - A special circuit inside Tx periodically checks for the presence of Rx load
  - Internal Rx-Detect output
To support Power Management
- Beacon => “Wake Up” call while in powerdown
- Special circuit in Tx for Beacon Transmit & in Rx for Beacon Detect
- Operate from $V_{DDAUX}$ supply

Example PMA Block Diagram

- Allows future BW headroom e.g. Next Gen PCI Exp link at 5 Gbps
- PMA has special features to support Hot-Plug, Power Mgmt. making it suitable for Mainstream applications
Elastic Buffer (RefClk +300 ppm)

System 1

Clk1
(100 MHz + 30KHz)

@ 2.50075 Gb/s

Recovered Clk = RefClk + 75 KHz

System 2

Clk 2
(100MHz)

@ 2.5Gb/s

Elastic Buffer

Elastic Buffer (RefClk -300 ppm)

System 1

Clk1
(100 MHz - 30KHz)

@ 2.49925 Gb/s

Recovered Clk = RefClk - 30 KHz

System 2

Clk 2
(100MHz)

@ 2.5Gb/s

Elastic Buffer
Elastic Buffer Mech. (Skip Sequence)

Data Packet 1 Skip Sequence Data Packet

Add Skip (Local RefClk > Remote RefClk)

Delete Skip (Local RefClk < Remote RefClk)

Data Flow

Lane de-skewing Function

- Done in MAC layer – to accommodate variable lane-width feature of PCI Express (e.g. x1, x4, etc)

During Init. Rd Ptrs. In MAC for each lane are set appropriately so that D[0] bytes for all lanes are read simultaneously
Putting it all together

Measurement to PCI Express Mask

- Separate tests used as a way of testing EQ
- How will we test more complicated EQ?
  - This was pretty darn simple