Announcements

- Homework #2 due next week
- Project will be posted this week
Outline

- PLL and DLL components
- Introduction to Viterbi decoder

Additional PLL material:
  - ISSCC’04 tutorial by Dennis Fischette
    http://www.delroy.com
  - References posted on the web
  - Chapter 12 in the textbook

Loop Components

- Phase Comparator
  - Produces UP/DN pulses corresponding to phase difference
- Charge Pump
  - Sources/sinks current for duration of UP/DN pulses
- Loop Filter
  - Integrates current to produce control voltage
- Voltage-Controlled Delay Line
  - Changes delay proportionally to voltage
- Voltage-Controlled Oscillator
  - Generates frequency proportional to control voltage
### Timing Loop Components

- **Phase Comparator**
  - measures the time difference between two signal transitions
  - for periodic signals measures the phase of one signal with respect to the other
  - the sensor for most timing loops

- **Delay Lines**
  - adjust the delay between two points in a system
  - the actuator for most timing loops
  - except for PLLs that use VCOs

- **Loop Filters**
  - smooth response of the timing loop
  - stabilize the loop (for PLLs)

[Dally]

### Phase Comparators

- **Output describes phase difference between two inputs**
  - may be analog or digital
  - may linearly cover a wide range, or just a narrow phase difference

[Dally]
**XOR Phase Detector**

- Sensitive to duty cycle

![Diagram of XOR Phase Detector](image)

**Flip-Flop Phase Comparator**

- Feed $\phi_1$ into the clock input
- Feed $\phi_2$ into the data input
- With single-edge triggered FF, if $Q$ is low, $\phi_1$ is ________.
- Note that when $\Delta \phi = 0$, FF is put in a metastable state
- If same FF used for receiver and phase comparator, aperture offset is compensated for.
- Bang-bang loop control
Other Phase Comparators

- Sequential phase-only comparator
  - asynchronous state machine
  - pulses “up” or “down” output from transition on one input to transition on the other

- Sequential phase-frequency comparator
  - like the sequential phase-only comparator
  - but also keeps track of number of transitions on the two inputs and attempts to make them equal
  - don’t use this for a DLL!!!

Phase-Frequency Detector

- Schematic

- State-transition diagram
## Dead-Zone in PFD

“Dead-zone” occurs when the loop doesn’t respond to small phase errors - e.g. 10 ps phase error at PFD inputs:

- PFD cannot generate 10 ps wide *Up* and *Down* pulses
- Charge-pump switches cannot turn on and off in 10 ps
- Solution: delay reset to guarantee min. pulse width (typically > 150 ps)

[Fischette]

## Charge Pump

- Converts PFD digital *Up/Down* signals into charge
- Charge is proportional to duration of *Up/Down* signals
  \[ Q_{cp} = I_{up} \cdot t_{up} - I_{dn} \cdot t_{dn} \]
- The LPF converts integrates currents
- Charge pump requirements:
  - Match currents \( I_{up} \) and \( I_{dn} \)
  - Reduce control voltage coupling
  - Supply noise rejection, PVT insensitivity
  (Simple or bandgap biased)
Charge Pump: Better Switches

- Unity-gain buffer controls the voltage over switches
- Current mirrored into $I_{up}/I_{dn}$

Young, JSSC 12/92

Charge Pump: Reversed Switches

Ingino, JSSC 11/01
Loop Filter

- Integrates charge-pump current onto $C_1$ cap to set average VCO frequency ("integral" path).
- Resistor provides instantaneous phase correction w/o affecting avg. freq. ("proportional" path).
- $C_2$ cap smooths IR ripple on $V_{ctl}$
- Typical value $R_{lpf}$ in kΩ

Loop Filter: Dual CP

- Transformation into PI

- Dual charge pump architecture
Low-Pass Filter Smoothing Cap ($C_3$)

- “Smoothing” capacitor on control voltage filters CP ripple, but may make loop unstable
- Creates parasitic pole: $\sigma_p = 1/(R C_2)$
- $C_3 < 1/10C_1$ for stability
- $C_3 > 1/50C_1$ for low jitter
- Smoothing cap reduces “IR”-induced VCO jitter to < 0.5% from 5-10%
- $\Delta f_{vco} = K_{vco}I_{cp} T_{err}/C_3$
- Larger $C_3/C_1$ increases phase error slightly

Fischette, ISSCC’04

Filter Capacitors

- Traditionally thin gate capacitance has been used
  - Below 130nm gate leakage is a problem
  - $C1$ in the range of tens of pF
- Alternative: thick oxide or metal cap
  - Area penalty
Variable Delay Elements

- Need:
  - a delay element
  - a method to vary the delay

- Delay elements
  - inverter
  - source-coupled amplifier

- Methods to vary delay
  - multiplexing a tapped delay line
  - varying the power supply to an inverter chain
  - varying the capacitance driven by each stage
  - varying the resistive load of a source-coupled amplifier

- Characterized by
  - max and min delay
  - typically a 2:1 throw
  - stability (jitter)

Single-ended vs. differential

- In CMOS inverter 1% of change in supply changes the delay by 1%
  (keep this in mind when using clock buffering)

- Current starved inverters and RC-loaded inverters are worse than 1%-for-1%.

- Improve by adding stabilization
Example VCO

- Ring-oscillator-based VCO: RC loaded

Regulated Delay Line

- Sidiropoulos'00
VCO: simple differential delay

- Change current
- Or better: Resistances
- Need linear, variable resistors

![VCO Diagram]

Delay Elements

- Maneatis, JSSC’95

![Delay Elements Diagram]
Replica Bias for the Delay Element

- Replica biasing improves supply and substrate rejection

Interpolation: Place an edge in between two existing edges

0.2\%delay/\%supply
Horowitz, IEEE Micro’98
Viterbi Algorithm

- Example of dynamic programming [Bellman'57]
- Invented by A. Viterbi in 1967
- Explained by Forney in 1972, 1973
- Used for:
  - Decoding convolutional codes
  - Decoding trellis codes
  - Maximum likelihood detection
  - Speech recognition, etc.
- Types:
  - Hard-input, hard-output
  - Soft-input, hard-output
  - Soft-input, soft-output
Trellis

- States + edges
- No loops
- Weights in minutes

Shortest Time to Get to Berkeley?

- What is the best path to take to:
  - Union City?
  - Hayward?

- Choose the minimum cost at each point (state)
Shortest Time to Get to Berkeley?

What is the best path to take to:
- Union City?

What is the best path to take to:
- Hayward?
Shortest Time to Get to Berkeley?

The Viterbi Algorithm

Illustrated by 2-state trellis

\[ sm_{n} = \min \left( sm_{n-1} + bm_{1}, \; sm_{n-1} + bm_{3} \right) \]
\[ sm_{n} = \min \left( sm_{n-1} + bm_{2}, \; sm_{n-1} + bm_{4} \right) \]
**Digital Baseband Transceiver**

- From channel (VCO)
- Low-Pass Filter
- ADC
- FIR Filter
- Detector
- (Viterbi Decoder)
- Data Postprocessor
- Timing Recovery
- Serial/Parallel
- Sync Detection
- Decoder
- Descrambler
- ECC Decoder
- ECC Encoder
- Data Interface

**Convolutional Codes**

- **Adding redundancy**
  - \( d_i \)
  - \( d_{i+1} \)
  - \( d_{i+2} \)
  - \( 1+D^2 \)
  - \( 0110 \)
  - \( 0100 \)
  - \( 0111 \)
  - Channel: \( (00, 11, 10, 10) \)

- **Generators:**
  - \( G_1 = 101 \)
  - \( G_2 = 111 \)
State Transition Diagrams