Outline

- Viterbi decoders
  - Very fast digital implementations
  - Analog implementations
- Decision-feedback equalizers
  - Operation
  - Digital implementations
  - Mixed-signal implementations
Extreme ACSs

- LSB-first computation
- MSB-first computation

Fettweiss, Meyr, TCom'90
Yeung, Rabaey, ISSCC'95
Drawings by Haratsch

RNS-Based ACS

\[ S = \sum_{i=0}^{w-1} s_i 2^i \]

\( s_i \in \{0, 1, 2\} \), and are two-bit encoded as \( s_i \in \{00, 01, 11\} \)
Bit-Level Pipelined ACS

Yeung, Rabaey, ISSCC'95

Radix-4 Redundant ACS

Yeung, Rabaey, ISSCC'95
Radix-4 ACS Bit Slice

Yeung, Rabaey, ISSCC'95

Analog ACS

Fukahori, ISSCC'98
Interleaved Analog ACS

Fukahori, ISSCC'98
Metric Normalization

State metrics $sm_i$ and $sm_j$ represented on a number circle

Survivor Path Decode

4-state trellis example
Survivor Path Decode

Register Exchange
Sliding Block Decoders

Black, Meng, JSSC'97

Receive Linear Equalizer

- Amplifies high-frequencies attenuated by the channel
- Pre-decision
- Digital or Analog FIR filter
- Issues
  - Also amplifies noise!
  - Precision
  - Tuning delays (if analog)
  - Setting coefficients
    - Adaptive algorithms such as LMS

H(s)

freq
### Linear Equalizer

- Equalizer cancels out ISI

![Linear Equalizer Diagram]

### Decision Feedback Equalizer

- Nonlinear equalizer

![Decision Feedback Equalizer Diagram]
DFE Block Diagram

Inter-Symbol Interference

Cursor

Pre-cursor ISI  Post-cursor ISI
Decision Feedback Equalization

- Don’t invert channel… just remove ISI
  - Know ISI because already received symbols
  - Doesn’t amplify noise
  - Has error accumulation problem
    - Less of an issue in links where random noise small
- Requires a feed-forward equalizer for precursor ISI
  - Reshapes pulse to eliminate precursor

DFE Operation

Brown, ISSCC’97
Error Propagation in DFE

- Decision errors at the output of the slicer can cause a corrupted estimate of the postcursor ISI by the postcursor equalizer.
- A single error can propagate indefinitely
  - This is a major concern in some applications
- Tomlinson-Harashima precoding can avoid it
- High-speed links operate with high SNR, and the probability is small

Receive Equalization

- Feedback equalization (DFE)
  - Subtracts error from input
  - No attenuation
- Problem with DFE
  - Need to know values of interfering bits
  - ISI must be causal
    - And latency in the decision circuit is a problem
    - Receive latency + DAC settling < bit time
  - Can increase allowable time by loop unrolling
    - Receive next bit before the previous is resolved
DFE Implementation

- **Digital implementation**
  - Requires front-end ADC
  - Architectural choices follow the structure of FIR filters
  - There is a feedback loop in the postcursor filter – loop unrolling

- **Mixed-signal implementations**
  - Voltage-domain implementations (DAC, RAM-based)
  - Current domain summation
  - Loop unrolling

Mixed-Signal DFEs

- **Direct DFE**
  - Mostly analog

- **Transpose DFE**
  - Mostly digital
Mixed-Signal DFE

Input

7th-order Linear-Phase LPF

\[ x'(t) \quad x(t) \]

\[ \alpha_0 \]

\[ \alpha_1 \]

\[ \text{FE Out} \]

kT

e_k

from DFE

Integrator

Integrator

RAM-Based DFE

\[ \Sigma \]

Postcursor ISI

\[ \hat{a}_{k-4} \quad \hat{a}_{k-3} \quad \hat{a}_{k-2} \quad \hat{a}_{k-1} \]

\[ Z^{-1} \quad Z^{-1} \quad Z^{-1} \quad Z^{-1} \]

\[ R(0000) \quad 0 \quad 0 \quad 0 \quad 0 \]

\[ R(1111) \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \]

- Four post-cursor estimates \( (a_{k-1} - a_{k-4}) \)
- New \( R(\text{Address}) = \text{old} \ R(\text{Address}) + \mu e_k \)

Brown, ISSCC’97
RAM-DFE

Mixed-Signal DFE

Brown, ISSCC’97

Le, JSSC’02
Current-Mode DFE

Instead of subtracting the error
- Move the slicer level to include the noise
- Slice for each possible level, since previous value unknown
Loop Unrolling Implementation

Offset slicer levels by +/- \( \alpha \)
- Previous symbol selects correct value
- \( M \) receivers for \( L \) taps, \( M \) level signal
- Each receiver with \( M-1 \) comparators

Look-ahead DFE

Kajley, JSSC’97
Look-ahead DFE

Putting It All Together

To compare different designs
- Compare the voltage margin at given BER

Need to include all noise sources
- Accurate ISI distribution
- Transmit and receive jitter
- CDR jitter
- EQ quantization noise
- Receiver offset

Stojanovic, CICC’03
BER Contours

5 tap Tx Eq

5 tap Tx Eq + 1 tap DFE

› Voltage margin
  › Min. distance between the receiver threshold and contours with same BER