Agenda

- Backplane channel review
- Link system models and noise
- Performance analysis
Backplane Environment - Recap

- Line attenuation
- Reflections from stubs (vias)

Backplane Channel

- Loss is variable
  - Same backplane
  - Different lengths
  - Different stubs
    - Top vs. Bot
- Required signal amplitude set by noise
- Need to architect the link to work over all channels
  - Need tools to estimate link performance over all channels
Inter-symbol Interference (ISI) - Recap

- Channel is low pass
  - Our nice short pulse gets spread out

- Dispersion – short latency (skin-effect, dielectric loss)
- Reflections – long latency (impedance mismatches – connectors, via stubs, device parasitics, package)

![Pulse response graph](image)

T_{symbol} = 160\text{ps}

ISI

- Middle sample is corrupted by 0.2 trailing ISI (from the previous symbol), and 0.1 leading ISI (from the next symbol) resulting in 0.3 total ISI
- As a result middle symbol is detected in error
Crosstalk

- Don’t just receive the signal you want
  - Get versions of signals “close” to you
  - Vertical connections have worse coupling
    - “Close” in these vertical connection regions

Frequency View of Crosstalk

- For this example:
  - > 4GHz, noise is as large as the signal
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  - Previous standard approaches
  - Statistical modeling
- Performance analysis

Parameter Definition for VT Based Budget

- Voltage parameter definitions
  - Simultaneous switching output (SSO) noise
  - Receiver sensitivity (offset + overdrive)
  - Channel loss
  - Crosstalk
  - Back-to-back read
- Timing parameter definitions
  - tQ: transmitter output timing
  - tSH: receiver output timing
  - tCE: channel timing error
  - tJ: clock source jitter
RDRAM VT Budget

<table>
<thead>
<tr>
<th>Component of Timing Budget</th>
<th>RAC to RDRAM ps</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit time</td>
<td>1250.0</td>
<td></td>
</tr>
<tr>
<td>RAC tQ</td>
<td>500.0</td>
<td>40.0%</td>
</tr>
<tr>
<td>RDRAM tSH</td>
<td>400.0</td>
<td>32.0%</td>
</tr>
<tr>
<td>tCE</td>
<td>290.0</td>
<td>23.2%</td>
</tr>
<tr>
<td>tJ</td>
<td>60.0</td>
<td>4.8%</td>
</tr>
<tr>
<td>Margin</td>
<td>0.0</td>
<td>0.0%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>100.0%</strong></td>
<td></td>
</tr>
</tbody>
</table>

- Vterm=1.2V and 36D (channel)
- At 800Mb/s
  - tCE is at 23% of bit time
  - vCE is at 62.5% Vswing (900mV)

Fiber Channel – Methodologies for Jitter Specification

- Total jitter = Deterministic (DJ) + random jitter (RJ)
- DJ: Non-Gaussian, bounded in amplitude and has specific causes (duty cycle distortion, data dependent, sinusoidal and uncorrelated (power supply noise injection))
- DJ is measured as a peak-to-peak value and adds linearly
- RJ: Gaussian and measured as an RMS value
- RJ: Peak-to-peak jitter = 14 * RMS jitter for a BER of 10^{-12}
- Total jitter = peak-to-peak DJ + peak-to-peak RJ
- Jitter measurement definitions
  - Jitter output
  - Jitter transfer
  - Jitter tolerance (ability of a CDR to successfully recover the data in the presence of jitter)
    - Create a tolerance mask by examining the CDR lock at different frequencies vs. sinusoidal jitter magnitude
Jitter measurement definitions

- Jitter generation (jitter added by the PLL due to phase and supply noise)
- Jitter transfer (jitter at the output of the PLL due to refClk noise)
- Jitter tolerance (ability of a CDR to successfully recover the data in the presence of jitter)
  - Create a tolerance mask by examining the CDR lock at different frequencies vs. sinusoidal jitter magnitude

Fiber Channel Jitter Specification for 1.0625 Gbps

<table>
<thead>
<tr>
<th>Variant</th>
<th>tr/f(ns)</th>
<th>Jitter (Unit Interval - UI)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S</td>
<td>R</td>
</tr>
<tr>
<td>100-SM-LL-L</td>
<td>0.37</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.08</td>
<td>Total</td>
</tr>
<tr>
<td>100-M5-SL-L</td>
<td>0.37</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100-TV-EL-S</td>
<td>0.4</td>
<td>0.7</td>
</tr>
<tr>
<td>100-MI-EL-S</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Previous system models

- Mostly non-existent
- Borrowed from computer systems
  - Worst case analysis
    - Can be too pessimistic in links
  - Gaussian distributions
    - Works well near mean
    - Often way off at tails
    - ISI distribution is bounded
- Borrowed from data communications
- Need accurate models
  - To relate the power/complexity to performance

Comparison w/ Gaussian Model

- Cumulative ISI distribution
- Impact on CDR phase

  - Gaussian model only good down to $10^{-3}$ probability
  - Way pessimistic for much lower probabilities
A new model

- Use direct noise and interference statistics
- Main system impairments
  - Interference
  - Voltage noise (thermal, supply, offsets, quantization)
  - Timing noise – always looked at separately
    - Key to integrate with voltage noise sources
    - Need to map from time to voltage

Residual ISI Error

- Cannot correct all the ISI
  - Equalizers are finite length
  - EQ coefficients quantized
  - Channel estimate error
- The error affects both voltage and timing
- Need to find the distribution of this error
Generating ISI Distributions

Convolution method

Tx Equalized pulse response

ISI distribution

Data sample distribution  Edge sample distribution

Estimated Residual Error

5 Tap Transmitter Equalizer
Equalizer Related Error Sources

- Residual ISI is the biggest source of error
- Quantization error and equalizer estimation
  - Are significant for reasonable assumptions about accuracy

Random Voltage Noise

- Thermal noise
  - Resistor and Device noise
- Quantization
- Estimation error
- Supply noise
- Receiver offset
Effect of Timing Noise

- Need to map from time to voltage

Voltage noise when receiver clock is off

- The effect is going to depend on the size of the jitter, the input sequence, and the channel

Effect of Transmitter Jitter

Jittered pulse decomposition

- Decompose output into ideal and noise
- Noise are pulses at front and end of symbol
  - Width of pulse is equal to jitter

Transmitter Jitter Noise

Approximate the noise pulses with deltas
- Assuming jitter is much narrower than channel impulse response

Channel output
- Output with no jitter
- Response to the noise deltas

Jitter effect on voltage noise

Transmitter jitter
- High frequency (cycle-cycle) jitter is bad
  - Changes the energy (area) of the symbol
  - No correlation of noise sources that sum
- Low frequency jitter is less bad
  - Effectively shifts waveform
  - Correlated noise give partial cancellation

Receive jitter
- Modeled by shift of transmit sequence
- Same as low frequency transmitter jitter
**Jitter Propagation Model**

Channel bandwidth matters

If \( h(T/2) \) is small, the noise is small

\( h(nT+1/2) \) not small, many pulses add

\[
x_{ISI} (kT + \phi_i + \epsilon_k^{RX}) = \sum_{j=-\infty}^{\infty} b_{k-j} p(jT + \phi_j)
\]

\[
x_{jitter}(kT + \phi_i + \epsilon_k^{RX}) = \sum_{j=-\infty}^{\infty} b_{k-j} \left[ h(jT + T/2 + \phi_j) (\epsilon_k^{RX} - \epsilon_{k-j}^{RX}) - h(jT-T/2 + \phi_j) (\epsilon_k^{RX} - \epsilon_{k-j}^{RX}) \right]
\]

- **Channel bandwidth matters**
  - If \( h(T/2) \) is small, the noise is small
  - \( h(nT+1/2) \) not small, many pulses add

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**Voltage Noise From Jitter**

- **White jitter**
  - Noise from Tx much larger than from Rx jitter
  - From Rx jitter, noise is white
  - From Tx jitter, filtered by the channel

- **Y-axis is noise \( \sigma \) (in Volts)**
  - If the noise was white
  - \( \sigma = 10 \text{mV} \Rightarrow -40 \text{dBV} \)

- **Bandwidth of the jitter is critical**
  - It sets the magnitude of the noise created
Jitter Source From PLL Clocks

- Noise sources
  - Reference clock phase noise
  - VCO supply noise
  - Clock buffer supply noise

- Stationary phase-space model

Noise Transfer Functions

- Low-pass from reference (input clock)
- Band-pass from VCO supply
- High-pass from clock buffer supply

PLL supply noise

Total noise ~ 25mV peak-to-peak
3.7% of on-chip $V_{ddA}$ (quiet PLL supply)

Where is this noise coming from?


Noise Spectrum (1)

Deterministic noise frequency components:
- 200MHz - ASIC core operating frequency.
  - Noise on link supplies due to ground bounce.
- 400MHz - reference clock, some link logic.
- 4GHz - link data rate.
  - Data & edge clocks at 2GHz => 4GHz noise.
  - Tail current modulation in diff. pairs.
Noise Spectrum (2)

- Random noise mostly white.
- Low frequency peaking in $V_{dd}$ noise due to underdamped impedance of distribution network.
  - $V_{clk}$ distribution network more damped because of higher resistance.

2x Oversampled Bang-Bang CDR

- Generate early/late from $d_n, d_{n-1}, e_n$
- Simple 1st order loop, cancels receiver setup time
- Now need jitter on data Clk, not PLL output
Data Clk Noise

- Model phase selector and PLL
  - Base linear PLL jitter
  - Add non-linear phase selector noise from CDR
- **Model the CDR loop as a state machine**
  - The current phase position is the state
  - State transitions are caused by early/late
  - Jitter on input data and PLL means
    - Possible to be late and get early PD result
    - Often filter early/late to generate up/down


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Transition Probabilities

- **Example system:**
  - CDR loop
  - Residual ISI
    - At edge -30dBV
  - Desired phase
    - State = 133

- **On average move to correct position**
  - But probability of wrong movement is not small
  - Need to find probability of at each phase location
Bang-Bang CDR Statistical Model

- Need steady state probabilities of the states
  - Have the transition probabilities

- Iteratively apply transition probabilities (Markov chain)
  - Results will converge to a steady-state

Bang-Bang CDR Model

- Gives the probability distribution of phase
  - Which is the CDR jitter distribution
Noise and Interference Summary

- Many important sources of noise and interference
  - ISI, crosstalk, quantization, estimation, etc.
- Largest error comes from ISI
  - By factor of 10x
- Timing is noisy too
  - High frequency transmitter jitter is bad
  - CDR jitter needs to be considered
    - Especially if the data input is noisy
- What is the impact on performance?

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ISI and CDR Phase Distributions

- In ideal world, there would be only two dots
  - This plot shows how these dots spread out
- Vertical slice – ISI distribution per time offset
- Horizontal weight – CDR phase distribution

Putting It All Together

- To compare different designs
  - Compare the voltage margin at given BER
- Need to include all noise sources
  - Accurate ISI distribution
  - Transmit and receive jitter
  - CDR jitter
  - EQ quantization noise
  - Receiver offset
BER Contours

5 tap Tx Eq

5 tap Tx Eq + 1 tap DFE

» Voltage margin

» Min. distance between the receiver threshold and contours with same BER
Model and measurements

- PAM4, 3 taps of transmit equalization, 5Gb/s, 26” FR4 channel

Example channels

- Legacy (FR4) - lots of reflections
- Microwave engineered (NELCO)

V. Stojanović, A. Amirkhani, M. Horowitz, “Optimal Linear Precoding with Theoretical and Practical Data Rates in High-Speed Serial-Link Backplane Communication,” IEEE International Conference on Communications, June 2004
Capacity achieving bit loading

- Capacity is very big
- Practical rates lower
  - low target BER < 10^{-15}
  - peak power constraint
- Thermal noise – the smallest noise source

Capacity with link-specific noise

- Effective noise from phase noise
  - Proportional to signal energy
  - Decreases expected gains
- Still, capacity is much higher than data rates in today’s links (3Gb/s)
Multi-tone with integer bit loading

- Peak-power constraint introduces large gap penalty to capacity (can go around with coding, but too expensive)
- Still pretty high data rates

Multi-level: Offset and jitter are crucial

- To make better use of available bandwidth, need better circuits
- PAM2/PAM4 robust candidate for next generation links
Full ISI compensation too costly

Today’s links cannot afford to compensate all ISI
  ▶ Limits today’s maximum achievable data rates

Conclusions

▶ Backplane links limited by the channel
▶ ISI is large in baseband links
  ▶ Can’t completely compensate
    ▶ (At least not with reasonable area/power)
  ▶ Residual ISI also increases CDR jitter
▶ Generally have low BER requirements
  ▶ Accurate noise statistic important
  ▶ Many of large noise source are bounded
▶ Power constrained transmitter
  ▶ PAM4 and PAM2 with simple DFE are attractive solutions
▶ Still, capacity of these links is very big
  ▶ Smart multi-tone?