Announcements

- Homework #3 (the last one!) posted, due in 10 days
- Feedback on project, e-mailed to you today
Outline

- Wrap up Ethernet
- Disk-drive signal processing

‘Marvel of Technology’
### Disk Drives

- 1956 IBM engineers in San Jose introduced the first computer disk storage system.
- The 305 RAMAC (Random Access Method of Accounting and Control) could store five million characters (five megabytes) of data on 50 disks, each 24 inches in diameter.

### Today’s Disks

- **Hitachi (IBM) Travelstar 70 Gb/in²**
- Experimental densities: 100+Gb/in²; every square inch of disk space could hold 12 GB – nearly as much data as a three 5.25-inch diameter DVD-ROMs. (4.7 GB per surface) or 20 CD-ROMs (each 650 MB).
- Desktop drives 300 GB
- Notebook drives 80 GB
- Microdrive (1-inch) > 4 GB.
**Trends in Magnetic Disk Drives**

Exponential growth in capacity is due to:
- Reduction of head flying height
- Reduction of the gap size in the head
- Reduction of the media thickness
- Advanced signal processing methods
- Advanced digital integrated circuits

**Areal density of data in disk drives:**

![Graph showing areal density of data from 1985 to 2005](http://www.storage.ibm.com/technolo/grochows/grocho01.htm)

**IBM’s Areal Densities**

![Graph showing IBM areal density perspective](http://www.storage.ibm.com/technolo/grochows/grocho01.htm)
Areal Density Trends

Data Rate Trends in Disk Drives

Source: ISSCC + vendors’ web sites
Flight Height

Rotation speeds: 4500 – 15000 rpm

Price Trends
Magnetic Recording Fundamentals

Magnetic Disk Track Recording

Magnetization Levels

Detected signal in the Head

Increased recording density results in:
- reduced peak amplitude
- peak shift

Reduced Amplitude

Isolated Pulses

Superposed Pulses

Peak Shift
Lorentzian Pulse

Lorentzian:

\[ s(t) = \frac{1}{1 + \left( \frac{2t}{PW_{50}} \right)^2} \]

Bandlimited Channels

- Spectral control (ISI control)
- SNR limitation
- Towards Shannon capacity

Equalization
- Partial response

Channel coding
- Trellis/Parity coding

Combined coding and Equalization
- Iterative coding

Going to 1Tb/in^2 density will lower the SNR by another 6dB
### Signal Equalization

- **Lorenzian Pulse**
  
  \[ I(t) = \frac{1}{1 + \left( \frac{2t}{PW_{50}} \right)^2} \]

- **Equalization** 
  
  \[ (1-D)(1+D)^n \]

**User density = \( PW_{50} / T \)**

- **PR4**
  
  \[ (1-D)(1+D) \]

- **EPR4**
  
  \[ (1-D)(1+D)^2 \]

- **E^2PR4**
  
  \[ (1-D)(1+D)^3 \]

### Signal Response

- **Simulated readback signal**

  **User density = 1.4**

  **User density = 3.0**
Amplitude Spectra

Equalization Targets
Read Channel Building Blocks

Eye Diagrams

PR4

EPR4
Maximum Likelihood Detection

The Viterbi Detector

<table>
<thead>
<tr>
<th>Equalization</th>
<th>Response</th>
<th>Memory</th>
<th>States</th>
</tr>
</thead>
<tbody>
<tr>
<td>PR4</td>
<td>1−D²</td>
<td>2</td>
<td>4 (2)</td>
</tr>
<tr>
<td>EPR4</td>
<td>(1−D)(1+D)²</td>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td>E²PR4</td>
<td>(1−D)(1+D)³</td>
<td>4</td>
<td>16</td>
</tr>
</tbody>
</table>

Alternative is to use DFE; not used in practice because of error propagation
**Error Distances**

- Channel input error sequence:
  \[ e_x(D) = \hat{x}(D) - x(D) \]

- Channel output error sequence:
  \[ e_y(D) = \hat{y}(D) - y(D) \]

- Squared Euclidean error distance:
  \[ d^2(E) = \|e_y(D)\|^2 = \|e_x(D)h(D)\|^2 \]

**Error Probability**

- Probability of misdetection of sequence \( S_k \) by \( S_k' \) is a function of error distance, \( d_k \)
- Performance of the PRML system is determined by the minimum distance error events

\[ P_e \approx K d_{\min} Q\left(\frac{d_{\min}}{2\sigma}\right) \]

- Error event distance spectrum
- \( Q() \) - Error function
**Signal Processing Trends**

![Signal Processing Trends Diagram]

**Current Implementation Approaches**

<table>
<thead>
<tr>
<th>Function</th>
<th>Approach</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Architecture</td>
<td>EPR, E’PR, or generalized E’PR with 16/17 or 8/9 codes</td>
</tr>
<tr>
<td>Equalization</td>
<td>Digital FIR, analog FIR, or continuous-time filter</td>
</tr>
<tr>
<td>ADC</td>
<td>Flash, typically 6 bits</td>
</tr>
<tr>
<td>Detection</td>
<td>Full Viterbi detector or Viterbi detector with post-processor</td>
</tr>
<tr>
<td>Gain control</td>
<td>First-order loop with digital or analog integration</td>
</tr>
<tr>
<td>Timing Recovery</td>
<td>Second-order PLL using synchronous or interpolated timing</td>
</tr>
</tbody>
</table>
Parity-Coded Channel

Architecture #1

Key Features:
• All analog

SSI, ’90-'97
Architecture #2

Key Features:
• Analog FIR equalizer
• 40-levels in ADC

Dominant:
Lucent

Architecture #3

Key Features:
• Digital FIR equalizer
• Full 6-bit ADC

Dominant:
TI (SSI), Marvell, Datapath, IBM
Architecture #4

Key Features:
- Digital FIR equalizer
- Interpolated timing recovery
- Full 6-bit ADC with >(1/T) samples/sec.

Design Examples

1st generation chip
170 Mb/s, 1.3W, 5V, 27.5mm², 0.56mm
Published in 1997 ISSCC Paper 19.7

2nd generation chip
240 Mb/s, 1.4W, 5V, 18.5mm², 0.54mm
Unpublished

3rd generation chip
400 Mb/s, 1.1W, 3.3V, 13.5mm², 0.29mm
Published in 1999 ISSCC Paper 2.2

Analog Front-End

- Pre-equalization in analog domain

Design Challenges

- One of the first Systems-on-a-Chip (SoC)
- > 2Gb/s rate
- Power limited (<2W, preferably 1W), inexpensive (<$2.5)
- Single step vs. lookahead/parallel
- Reduced SNR, complex detection
- Integration with controller gives opportunities for more powerful coding and processing
- Iterative decoders (Turbo, LDPC)
Architectural Choices

» Equalizer
  - 6-10 taps, >1Gb/s
  - Choices of interleaving, pipelining, recoding, carry-save
  - “Infinite” speed at the expense of power

Architectural Choices

» Viterbi Decoder
  - 16 – 32 state, trellis coded with prostprocessor, variable equalization targets
  - Radix-2 vs. Radix-4, ACS vs. CSA
  - Bit-level pipelining
Future Signal Processing

- SNRs will continue to decrease
- Iterative decoding – LDPC based
  - Can we control the byte error rate?
  - Complexity?
  - Timing recovery at low SNRs
- Vertical recording is already back
- Multi-track recording?

IBM’s Advanced Storage Roadmap
Holographic Storage

IBM's Millipede