EE290C - Spring 2004
Advanced Topics in Circuit Design
High-Speed Electrical Interfaces

Lecture #7
Components
  Termination, Transmitters & Receivers
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2/10/04

Outline

- General issues
- Termination
- Transmitters
- Receivers
General Issues

- Single-ended vs. Differential
- Voltage mode vs. current mode
- I/O clocking & use of phasors
- RiCi

Single-ended vs. Differential

- Single-ended signaling – compare to shared reference
  - Often used with a bus
- Issues
  - Generates SSO noise
  - How to make reference
  - How to quiet reference: difference in bypass network if shared
  - Crosstalk cannot be made common-mode
- Differential must run > 2x as fast as single-ended to make sense
  - Often debated if this always can be done
Voltage mode vs. current mode

- In a transmission-line environment does this terminology make sense?
  - A wave has voltage and current, right?
- Answer is in the driver Z
  - Low Z driver = voltage mode
  - High Z driver = current mode

Clock Frequency Limits

- Min clock period > 8-FO4 (i.e. 1-GHz @ 0.25u)
- Faster links should use multiple clocks:
  - Critical on mux/demux
I/O clocking & use of phasors

- Heavy multiplexing of input & output data streams allows for performance higher than process technology would seem to allow
  - Can get out of hand

RiCi & Pad Complexity

- You can’t just add arbitrary complexity at the pad
- Tx, Rx, ESD & Pad itself have RiCi which makes pole
- In multi-drop busses, multiple poles at same frequency can stack up!
Termination

- Why terminate?
- External vs. internal
- Series vs. Parallel
- AC vs. DC termination
- Untrimmed poly
- Active termination

Why terminate?

- Termination keeps energy from bouncing around
- In current-mode signaling voltage is developed across the terminator
- Quality of termination can limit system performance
**External vs. Internal**

- + Internal termination makes package L part of T-line
- + Eliminates package as ‘stub’
- - Increases complexity, poor tolerances for on-die R's

**Series vs. Parallel Termination**

- Series often used with voltage mode
  - Driver lower Z than Rt
- Parallel with current-mode
  - Driver higher Z than Rt
- Driver Z hard to control across PVT
  - Highest performance is usually through parallel termination
AC vs. DC Termination

- With differential signals can terminate to the compliment
  - Potential power savings
  - Can build a higher-Z system
  - What sets common-mode?
    - Usually TX
    - Demands large RX common-mode range
  - AC-coupled & AC-term
    - Now can set common mode with parallel large R’s

Termination With Untrimmed Poly

- Issue is variation in sheet resistance & C_D
- Typically +/- 15% in sheet-rho at one temperature
- Also typically varies with temperature
- BUT
  - At least it’s always a resistor (no non-linearities)
  - It’s simple
  - It’s ESD robust
Active Termination

- (a) Triode
- (b) Two-Element
- (c) Pass-Gate
- (d) Digital Trimming

IV-characteristic of two-element resistor

Termination Example: SSTL Source

Conventional CMOS Signaling:
- 1.5V
- 25Ω
- 0.1 ns, ZO=50 Ω
- 6.5pF
- P_{term} = 40 mW (two term/s)
- P_{dx} = 60 mW

SSTL-Style Signaling:
- 1.5V
- 25Ω
- 40Ω
- 40Ω
- V_{RFL} = V_T
- P_{term} = 5 mW (2 term/s)
- P_{dx} = 12.5 mW

Series resistor isolates stub from line, increases line impedance, reduces ringing, reduces power

Better receiver and (slightly) better reference.
SSTL Conventional w/o source

1" stubs w/ 1" spacing

resolvers

$t=0.81 \text{ ns}$

SSTL - with source damping resistors

Resistors act like rubber bands

$Rs=Zo/2$

receivers

$t=0.81 \text{ ns}$
RSL: Compensated short stubs

Memory reads split 50/50 and go in each direction
Then double at the master end to restore full-swing
Writes go straight through to terminator
Allows for multi-drop memory bus with high-Z drivers
Transmitters

- Single-ended
  - SSTL
  - RSL
  - GTL
- Differential
  - LVDS
  - CML
- Transmitter timing
- Other TX Design Issues

Tx Single-ended

- Classic inverter... why not?
  - Poor Z matching at Tx; very prone to reflections
  - Generates extreme amounts of SSO noise
    - Easily order(Vdd) if there is any L and large # of drivers
  - Have to generate term voltage at Rx; burns power
Single-Ended : SSTL

Class-I

\[ I_o = +/ - 8\, \text{mA} \]

\[ V_{\text{TT}} = \frac{1}{2} V_{\text{DDQ}} \] (center term)

Class-II

\[ I_o = +/ - 16\, \text{mA} \]

\[ V_{\text{TT}} = \frac{1}{2} V_{\text{DDQ}} \] (center term)

Single-Ended : SSTL characteristics

- Center-terminated, push-pull
- Very flexible termination
  - Allows double, single, or no termination
  - But source term slows edge rates & limits speed
- Very simple
  - Driver can be simple inverter
  - Receiver can be simple inverter

... but PVT varying output driver means reflections
Single-Ended : RSL

Open drain current-source driver
- Current-control to keep constant i over PVT
- Slew-rate control to keep rate low enough to avoid overshoot & ringing
- Low-swing with reference
- Relatively expensive and complicated

Very short stubs
- Aggressive Ci, Li
- Tuned out with loaded/unload sections
Single-Ended : GTL/GTL+

- $I_o = -40\text{mA}$
- $V_{TT} = 1.2V$
- $V_{REF} = 0.8V$
- $Z_0 = 50\Omega$

Single-Ended : GTL/GTL+ characteristics

- “Just like Rambus”
- But... output driver goes linear
  - No current-control
  - Resistance presents Z-discontinuity to line
- Lower Vterm doesn’t help transmitter Ron
  - Addressed somewhat in GTL+ which shifted term
**Differential : LVDS**

- $I_o = +/- 3.5\text{mA}$
- $V_{CM} = 1.25\text{V}$ (set by driver)
- $Z_o = 100\Omega$
- AC terminated @ receiver

**Differential : LVDS characteristics**

- **Differential**
  - Eliminates non-common mode reference noise
  - Also (ideally) keeps current at driver constant
  - Low power - only $+/- 3.5\text{mA}$

- **Termination at the RX on-chip or off**
  - No references, can ship across cable
  - Requires very wide CM range from RX
  - Unterminated at driver; reflections occur from discontinuities
  - Timing of driver push-pull ckt can be a challenge
**Differential : CML - direct coupled**

\[ I_o = -21 mA \]

\[ Z_o = 50 \Omega \]

Double-terminated on-chip

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**Differential : CML - AC coupled**

\[ I_o = -21 mA \]

Supports different on-chip Vterms
Differential: CML Characteristics

- **Open-drain**
  - High common-mode keeps saturation
- **DC or AC coupled**
  - AC-coupling requires 8b10b coding
- **Termination**
  - DC-term: Better control of CM than LVDS
  - Requires on-chip term network
  - Double-terminated
    - Minimize reflections off driver
    - Driver and receiver both see 25Ω
    - More power
      - 4x LVDS just from 100Ω -> 25Ω term

Physical signal swings

1. Swing @ receiver input, driver swing will be higher.
2. Differential signalling
Simple Transmitter Timing

- DDR: send a bit per clock edge
- Critical issues:
  - 50% duty cycle
  - Tbit > 4-FO4

Very Fast Transmitter Timing

- Off chip time constant smaller than on chip:
  - Generate current pulse at the output
  - Limited only by the output capacitance
  - Need to be very careful to match & tune; otherwise can make things worse

Limiting time constant 25-Ω*Cpad

Cpad = 8*Cdriver + Cesd
More TX Design Issues

- **Saturation Margin**
  - Drivers with current sources are limited in common-mode range
  - Must keep tail saturated; otherwise Z is thrown off

- **DC Distortion, ISI generation**
  - What drives the driver? How far back to get to CMOS levels?
  - It is easy to amplify errors by unknowingly biasing your circuit to a level or to an edge

- **Edge-rate Control**
  - At FF corner your TX can generate edge-rates too fast
    - Higher xtalk (especially NEXT)
    - More reflections (smaller Z discontinuities)

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Receivers

- **Basic receive architectures**
- **StrongARM latch & improved latch**
- **Single-ended : reference noise**
- **Integrating receivers**
- **RX Design Issues**
Two Basic Receive Architectures

- Amplify then sample or...
- Sample, then amplify

Rx Example: StrongARM Latch

- Simple single clock design
- Grey device show cross-coupled inverters that regenerate.
- Need a follow-on latch at the output to hold the data for the full clock cycle.
Rx Example: StrongARM Latch

- Has sampling noise and charge kickback from switching.
- Input offset not great: 50-100mV
- Bit-time is limited by the cycle-time (to have enough gain)
- Common-mode gain effects through the tail device in linear region

Improved Sampling Receiver

- Improvements in common-mode sensitivity, kickback, offsets through correction port (loffP,loffM)
Receiver Evaluation: Step Response

- Can calculate pulse response of Rx front-end
- Indicates aperture & gain-bandwidth characteristics of the receiver
- Can be convolved with the channel response

Integrating Rx & Reference Noise

- Integrator used to mute the effect of high-frequency noise
  - Most interesting in single-ended systems
  - High frequency noise is often L*dl/dt switching noise on reference
  - Due to differences in loading between reference & signal
Integrating Receiver Design

Integrating Receiver Windowing

Integration time is windowed to match valid data & minimize anti-data
RX Design Issues

- **Offset**
  - Typically front-ends have 10-30mV of uncorrected offset
  - Heavy MonteCarlo sims and active methods must be used to reduce offsets to ~5mV in multi-receiver designs

- **Aperture**
  - Need Gain*BW
  - BW in slicer domain translates to pulse response width or aperture

- **ISI**
  - Must properly reset the receiver before the next evaluate phase
  - Often there is some residual ISI or negative ISI you must eat

- **Common-mode gain**
  - Most structures have different gain characteristics (and thus sensitivity) across the range of common-modes. Often end up restricting range or adding preamp

ISSCC 2004 Next Week

- Interesting sessions in high-speed I/O highlighted
- Be prepared to talk on at least 2 papers from these sessions