COPING WITH INTERCONNECT
Impact of Interconnect Parasitics

• Reduce Reliability
• Affect Performance

Classes of Parasitics

• Capacitive
• Resistive
• Inductive
Nature of Interconnect

\[ S_{\text{Local}} = S_{\text{Technology}} \]
\[ S_{\text{Global}} = S_{\text{Die}} \]
Dealing with Capacitance
Capacitance: The Parallel Plate Model

\[ C_{int} = \frac{\varepsilon_{ox} W}{t_{ox} L} \]

\[ S_{C,wire} = \frac{S \times S_L}{S} = S_L \]
## Typical Wiring Capacitance Values

<table>
<thead>
<tr>
<th>Interconnect Layer</th>
<th>fF/μm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polysilicon To Substrate</td>
<td>0.058 ± 0.004</td>
</tr>
<tr>
<td>Metal1 To Substrate</td>
<td>0.031 ± 0.001</td>
</tr>
<tr>
<td>Metal2 To Substrate</td>
<td>0.015 ± 0.001</td>
</tr>
<tr>
<td>Metal3 to Substrate</td>
<td>0.010 ± 0.001</td>
</tr>
<tr>
<td>N⁺ Diffusion To Substrate (@ 0 Volt)</td>
<td>0.36 ± 0.02</td>
</tr>
<tr>
<td>P⁺ Diffusion To Substrate (@ 0 Volt)</td>
<td>0.46 ± 0.06</td>
</tr>
</tbody>
</table>

Capacitance/Unit Area for Typical Interconnect Layers (1 μm CMOS)
Fringing Capacitance

\[ W - \frac{H}{2} \]

(a)

(b)
# Fringing Capacitance: Values

<table>
<thead>
<tr>
<th></th>
<th>Fringing Capacitance (fF/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polysilicon To Substrate</td>
<td>0.043 ± 0.004</td>
</tr>
<tr>
<td>Metal1 To Substrate</td>
<td>0.044 ± 0.001</td>
</tr>
<tr>
<td>Metal2 To Substrate</td>
<td>0.035 ± 0.001</td>
</tr>
<tr>
<td>Metal3 To Substrate</td>
<td>0.033 ± 0.001</td>
</tr>
</tbody>
</table>

Fringing Capacitance per Unit Length (for a 1 μm CMOS process).
How to counter Clock Skew?

(from [Bakoglu89])
Interwire Capacitance

Creates Cross-talk
# Interwire Capacitance

Inter-Wire Capacitance for 1 μm CMOS Process.

<table>
<thead>
<tr>
<th></th>
<th>Area Capacitance (fF/μm²)</th>
<th>Fringing Capacitance (fF/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal1 to Polysilicon</td>
<td>0.055</td>
<td>0.049</td>
</tr>
<tr>
<td>Metal2 to Polysilicon</td>
<td>0.022</td>
<td>0.040</td>
</tr>
<tr>
<td>Metal2 to Metal1</td>
<td>0.035</td>
<td>0.046</td>
</tr>
</tbody>
</table>
Impact of Interwire Capacitance

(from [Bakoglu89])
Capacitance Crosstalk

\[ V_{DD} \]

\[ \phi \]

\[ \text{PDN} \]

\[ C_{XY} \]

\[ X \]

\[ Y \]

\[ C_{X} \]

\[ 5V \]

\[ \text{Overlap: 0.35 V Interference} \]

\[ 5 \times 5 \mu m \]
How to Battle Capacitive Crosstalk

- Avoid parallel wires

- Shielding

![Diagram showing shielding and substrate connections]

- Shielding wire
- Substrate (GND)
- Ground (GND)
- Power supply (VDD)
- Shielding layer
Driving Large Capacitances

\[ t_{pHL} = C_L \frac{V_{swing}}{2} \]

Transistor Sizing
Using Cascaded Buffers

\[ u_{\text{opt}} = e \]
$t_p$ in function of $u$ and $x$
# Impact of Cascading Buffers

<table>
<thead>
<tr>
<th>$x$</th>
<th>Unbuffered</th>
<th>Single Buffer</th>
<th>Cascaded Buffers</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>10</td>
<td>6.3</td>
<td>6.3</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
<td>20</td>
<td>12.5</td>
</tr>
<tr>
<td>1000</td>
<td>1000</td>
<td>63</td>
<td>18.8</td>
</tr>
<tr>
<td>10,000</td>
<td>10,000</td>
<td>200</td>
<td>25.0</td>
</tr>
</tbody>
</table>

$t_{opt}/t_{p0}$ versus $x$ for various driver configurations.

$C_{in} = 10$ fF in 1 μm CMOS
# Output Driver Design

Driver for 20 pF Load

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_n$ (μm)</td>
<td>1.8</td>
<td>5.3</td>
<td>15.8</td>
<td>47.7</td>
<td>138.2</td>
<td>409.0</td>
<td>1210.7</td>
</tr>
<tr>
<td>$W_p$ (μm)</td>
<td>2.8</td>
<td>8.4</td>
<td>24.9</td>
<td>73.8</td>
<td>218.3</td>
<td>646.2</td>
<td>1912.8</td>
</tr>
</tbody>
</table>

Transistor sizes for optimally-sized cascaded buffers.

$t_p = 4.2$ ns

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_n$ (μm)</td>
<td>1.8</td>
<td>22.7</td>
<td>286.0</td>
</tr>
<tr>
<td>$W_p$ (μm)</td>
<td>2.8</td>
<td>35.3</td>
<td>444.5</td>
</tr>
</tbody>
</table>

Transistor Sizes of Optimized Cascaded Buffer.

$t_p = 7.6$ ns
How to Design Large Transistors

(a) small transistors in parallel

(b) circular transistors
Bonding Pad Design

Bonding Pad

V_{DD}  GND

In  Out

100 µm

GND

Out
Reducing the swing

\[ t_{\text{pHL}} = \frac{C_L}{I_{\text{av}}} \]

- Reducing the swing potentially yields linear reduction in delay
- Also results in reduction in power dissipation
- Requires use of “sense amplifier” to restore signal level
Charge Redistribution Amplifier

(a)
Precharged Bus

![Diagram of a precharged bus with transistors M1, M2, M3, and M4, and capacitors Cbus and Cout. The diagram includes waveforms for Vbus, Vsym, Vasymp, and f, with values for Cbus = 1pF.]
Tristate Buffers
Using Bipolar Versus MOS

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>Bipolar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current</td>
<td>$I_{DS} = \frac{Q_I}{\tau_T}$</td>
<td>$I_C = \frac{Q_F}{\tau_F}$</td>
</tr>
<tr>
<td>Charge</td>
<td>$Q_I \approx A_G(V_{GS}-V_T)$</td>
<td>$Q_F \approx A_E e^{\frac{V_{be}}{V_t}}$</td>
</tr>
<tr>
<td>Transit Time</td>
<td>$\tau_T = \frac{L}{V_{sat}}$</td>
<td>$\tau_F = \frac{W_b^2}{2D_b}$</td>
</tr>
</tbody>
</table>

Analysis of Driving Capabilities of CMOS and Bipolar Transistors.

But: Bipolar does not scale well with voltage!
Bipolar Versus MOS (cont.)

Driving a 10 pF Capacitance using Emitter(Source)-Followers
Dealing with Resistance
Wire Resistance

\[ R = \frac{\rho L}{H W} \]

Sheet Resistance \( R_0 \)

\[ R_1 \equiv R_2 \]
Interconnect Resistance

<table>
<thead>
<tr>
<th>Material</th>
<th>Sheet Resistance (Ω/□)</th>
</tr>
</thead>
<tbody>
<tr>
<td>n+ diffusion</td>
<td>10 ± 2</td>
</tr>
<tr>
<td>p+ diffusion</td>
<td>10 ± 2</td>
</tr>
<tr>
<td>n-well (under field)</td>
<td>1150 ± 250</td>
</tr>
<tr>
<td>polysilicon (H = 0.33μm)</td>
<td>10 ± 2</td>
</tr>
<tr>
<td>metal1, metal2</td>
<td>0.07 ± 0.006</td>
</tr>
</tbody>
</table>

Sheet Resistance Values for a Typical 1.0 μm CMOS process.

\[
R = R_{\square} \frac{L}{W}
\]

\[
S_R = S_{R_{\square}} \frac{S_L}{S}
\]

\[
S_{RC} = \frac{S_L^2}{S^2}
\]

\[
S_{\Delta V} = \frac{S_L}{S}
\]
Dealing with Resistance

• Selective Technology Scaling

• Use Better Interconnect Materials
e.g. silicides, bypasses

• More Interconnect Layers
reduce average wire-length
Polycide Gate Mosfet

Silicides: WSi$_2$, TiSi$_2$, PtSi$_2$ and TaSi

Conductivity: 8-10 times better than Poly
Modern Interconnect
RI Introduced Noise

\[ V_{DD} \quad I \quad R' \quad \phi_{pre} \quad \Delta V \quad I \quad R \]

\[ X \quad V_{DD} - \Delta V' \quad \Delta V \]
Power and Ground Distribution

(a) Finger-shaped network
(b) Network with multiple supply pins
Electromigration (1)

Limits dc-current to 1 mA/µm
Electromigration (2)
RC-Delay

\[ r_c \frac{\partial V}{\partial t} = \frac{2}{\partial x^2} \]

\[ \tau(V_{out}) = \frac{rc L^2}{2} \]
RC-Models

<table>
<thead>
<tr>
<th>Voltage Range</th>
<th>Lumped RC-network</th>
<th>Distributed RC-network</th>
</tr>
</thead>
<tbody>
<tr>
<td>0→50% ($t_p$)</td>
<td>0.69 RC</td>
<td>0.38 RC</td>
</tr>
<tr>
<td>0→63% ($\tau$)</td>
<td>RC</td>
<td>0.5 RC</td>
</tr>
<tr>
<td>10%→90% ($t_r$)</td>
<td>2.2 RC</td>
<td>0.9 RC</td>
</tr>
</tbody>
</table>

Step Response of Lumped and Distributed RC Networks:
Points of Interest.
Reducing RC-delay

Repeater

\[ M = L \sqrt{\frac{0.38rc}{t_{pbuf}}} \]
The Ellmore Delay

\[
\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j
\]
\[
\int_{0}^{\infty} v_i(t) dt = \sum_{k=1}^{N} C_k V_k(0) R_{i,k}
\]

with

\[
R_{i,k} = \sum_{j} R_j \Rightarrow \{ R_j \in [path(i \to r) \cap path(k \to r)] \}.
\]
INTERCONNECT

Dealing with Inductance
Inductive Effects in Integrated Circuits

Coaxial Cable

Triplate Strip Line

MicroStrip

Wire above Ground Plane
L di/ dt
L di/ dt: Simulation

Signals Waveforms for Output Driver connected To Bonding Pads

(a) $v_{out}$; (b) $i_L$ and (c) $v_L$.

The Results of an Actual Simulation are Shown on the Right Side.
Choosing the Right Pin

Make Rise- and Fall Times as slow as possible
Decoupling Capacitors

- Supply
- Bonding Wire
- Decoupling Capacitor
- CHIP
- Board Wiring
The Transmission Line

\[
\frac{2}{\partial x^2} = r c \frac{\partial v}{\partial t} + l c \frac{2}{\partial t^2} v
\]
Lossless Transmission Line - Parameters

Propagation Speed: Only a function of surrounding medium

\[ v = \frac{1}{\sqrt{tc}} = \frac{1}{\sqrt{\varepsilon\mu}} = \frac{c_0}{\sqrt{\varepsilon_r\mu_r}} \]

speed of light in vacuum

\[ t_f = \frac{1}{v} = \sqrt{tc} \]

\( \varepsilon \): permittivity of insulator

\( \mu \): permeability of insulator

Characteristic Impedance = Impedance presented by wire

\[ Z_0 = \sqrt{\frac{l}{c}} \]

100 to 500 \( \Omega \) for typical wires
# Wave Propagation Speed

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>$\varepsilon_r$</th>
<th>Propagation Speed (cm/nsec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vacuum</td>
<td>1</td>
<td>30</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>3.9</td>
<td>15</td>
</tr>
<tr>
<td>PC Board (Epoxy Glass)</td>
<td>5.0</td>
<td>13</td>
</tr>
<tr>
<td>Alumina (Ceramic Package)</td>
<td>9.5</td>
<td>10</td>
</tr>
</tbody>
</table>

Dielectric Constants and Wave Propagation Speeds for Various Materials, Used in Electronic Circuits (from [Bakoglu90]).
Wave Reflection for Different Terminations

Reflection Coefficient

\[ \rho = \frac{V_{\text{refl}}}{V_{\text{inc}}} = \frac{I_{\text{refl}}}{I_{\text{inc}}} = \frac{R - Z_0}{R + Z_0} \]
Transmission Line Response \((R_L = \infty)\)

\[ V_{\text{Source}} \]

(a) \(R_S = 5Z_0\)

(b) \(R_S = Z_0\)

(c) \(R_S = \frac{Z_0}{5}\)
ECL Gate Line Response

(a)
Output Buffer Model

(a)
Output Buffer - Response

\[ V_{in} \]

\[ V_{out} \]

\[ t \text{ (nsec)} \]

\[ C_L = 5\text{pF} \]

\[ R_L = 100\Omega \]

\[ C_L' = 25\text{pF} \]

\[ R_L = 100\Omega \]
When to Consider Transmission Line Effects?

- Transmission line effects should be considered when the rise or fall time of the input signal \((t_r, t_f)\) is smaller than the time-of-flight of the transmission line \((t_{flight})\).

**Rule of Thumb**

\[ t_r(t_f) < 2.5t_{flight} = 2.5 \frac{L}{v} \]
Packaging

Requirements

• Electrical: Low parasitics
• Mechanical: Reliable and Robust
• Thermal: Efficient Heat Removal
• Economical: Cheap
Bonding Techniques

Wire Bonding

Substrate

Die

Pad

Lead Frame
Tape-Automated Bonding (TAB)

(a) Polymer Tape with imprinted wiring pattern.

(b) Die attachment using solder bumps.
Flip-Chip Bonding

Die

Solder bumps

Substrate

Interconnect layers
Package-to-Board Interconnect

(a) Through-Hole Mounting

(b) Surface Mount
Package Types
## Package Parameters

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Capacitance (pF)</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>68 Pin Plastic DIP</td>
<td>4</td>
<td>35</td>
</tr>
<tr>
<td>68 Pin Ceramic DIP</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>256 Pin Pin Grid Array</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>Wire Bond</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Solder Bump</td>
<td>0.5</td>
<td>0.1</td>
</tr>
</tbody>
</table>

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])
Multi-Chip Modules