Problem 1: Static and dynamic analysis
Consider the following logic circuit:

\[ V_{out}(t=\infty) = V_{DD} - V_T(V_{out}) \]
\[ = 3 - (0.7 + 0.5(V_{out} + V_{out} - V_{dd})) \]

For solution

\[ V_{out}(t=\infty): 1.85V \]

b. Determine \( t_{PLH} \) at \( V_{out} \). Assume an ideal step at the input. The external load capacitance \( C_L \) can be assumed to be large and equals 10 pF.

\[ V_{swing} = 1.85V \rightarrow V_{so,50} = 0.95 \]
Transistor always in saturation!

\[ I(V_{out}=0) = \frac{1}{2} \cdot 10 \cdot 0.20 (3 - 0.75)^2 = 253 \mu A \]
\[ I(V_{out}=0.95) = \frac{1}{2} \cdot 5 \cdot 0.20 (3 - 0.95 - V_T)^2 = 61.6 \mu A \]
\[ V_T(V_{out}=0.95) = 0.84V \]
\[ I_{av} = \frac{(253 + 61.6)}/2 = 157.3 \mu A \]
\[ t_{PLH} = \frac{10 \text{ pF} \times 0.95}{157.3 \mu A} = 69 \text{ nsec} \]
c. Determine the energy that is stored on $C_L$ at the end of the low-to-high transition. How much energy was dissipated in the MOS transistor? How much was delivered by the input source? HINT: Derive the results; Do not take the equations in the book for granted!

$$E_{CL} = \frac{C_L V_{sw}^2}{2} = \frac{10\text{pF} \cdot 1.85^2}{2} = 17.9\text{pJ}$$

$$E_{vin} = C_L V_{sw} V_{dd} = 10 \times 1.85 \times 3 = 56.7\text{pJ}$$

$$E_{mos} = E_{vin} - E_{CL} = 28.3\text{pJ}$$

\[ E(C_L) = 17.9\text{pJ} \]
\[ E(MOS) = 38.3\text{pJ} \]
\[ E(V_{in}) = 56.7\text{pJ} \]

d. Assume that the NMOS is replaced by a PMOS device of the same size with its gate connected to GND. Determine the impact on the following design parameters, and give a short explanation.

**EXPLAIN:**

- $V_{out}(t = \infty)$:
  - Larger: PMOS charged all the way to $VDD \Rightarrow V_{out}(\infty) = 3V$
  - Equal: Not possible
  - Smaller: Not possible

- $t_{plh}$:
  - Larger: There is more current drive for PMOS (no body effect), get PMOS
  - Equal: Not possible
  - Smaller: Overall slower

- $E(V_{in})$:
  - Larger: Higher swing at the output
  - Equal: No change
  - Smaller: No change
e. Describe in a couple of sentences how you would decrease the delay of this gate. Is there an absolute lower limit on the delay, and if yes explain why and give an approximate value of this delay:

How would you reduce the delay?

Make transistor larger: \( \frac{w}{L} \text{NMOS} \)

Absolute minimum delay? Why?

At some point, intrinsic capacitance of NMOS becomes dominant > 10pF -> delay remains constant

Approximate value of minimum delay

The minimum delay is approximately equal to the delay of an unloaded minimum size inverter (tPO)
PROBLEM 2: MOS Capacitances

Consider the following simple circuit (implemented in the 1.2 μm CMOS technology). Assume $V_{DD} = 3$ V and use the following transistor parameters: $C_{ox} = 1.75 \text{ fF/μm}^2$, $x_j$ (lateral diffusion) = 0.15 μm, $C_j 0 = 3.0 \times 10^{-4} \text{ F/m}^2$, $m_j = 0.5$, $C_{jsw} = 8.0 \times 10^{-10} \text{ F/m}$, $m_{jsw} = 0.5$.

Assume that $V_G$ is initially at 0 V. We want to compute the time it will take to raise $V_G$ to $V_{DD}$. To do so, we will lump the device parasitic capacitances into a single lumped capacitance. This capacitance is a function of the operation region of the device.

(a) Determine the operation regions the MOS transistor is traversing during the transient (for $V_G$ going from 0 to $V_{DD}$).

Region 1: $V_G < V_T$

Region 2: $V_T < V_G < V_{DD}$

Region 3: ...

(b) Determine the (average) lumped capacitance seen at the gate of the MOS transistor in each of these regions.

**Cutoff:** $C_g = C_{ox} \cdot W \cdot L = 1.75 \times 3 \times 1.2 = 6.3 \text{ fF}$

**Saturation:**

\[
C_g = \frac{C_{ox} \cdot W \cdot L \cdot 0.5 \cdot \frac{2}{3}}{\text{overlap}}
\]

\[
= 1.75 \times 3 \times 0.3 + \frac{2}{3} \times 1.75 \times 3 \times 0.9
\]

\[
= 4.725 \text{ fF}
\]

\[
C_g (\text{region 1}): 6.3 \text{ fF}
\]

\[
C_g (\text{region 2}): 4.725 \text{ fF}
\]

\[
C_o (\text{region 3}): 
\]
c Determine the total time it will take for $V_G$ to go from 0 V to $V_{DD}$ (for $I_{in} = 100 \, \mu A$),

$$
t_1 = \frac{\Delta V \cdot C_G}{I} = \frac{0.75 \cdot 6.3 \mu F}{100 \, \mu A} = 47 \, \text{ps}
$$

$$
t_2 = \frac{(3 - 0.75) \cdot 4.725 \mu F}{100 \, \mu A} = 106.3 \, \text{ps}
$$

$$
t_{tot} = t_1 + t_2
$$

$t(0 \rightarrow V_{DD})$: 153 ps