This is an individual project; everybody should turn in a project report. More information on what to include in the report and how to submit your circuit will be available later.

**Design Objective**

The objective of this project is to design an operational amplifier having a differential input and a single ended output and with the following specifications:

<table>
<thead>
<tr>
<th>Process</th>
<th>0.13 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>1.2 V</td>
</tr>
<tr>
<td>$A_{dm}$</td>
<td>1000</td>
</tr>
<tr>
<td>$A_{cm}$</td>
<td>$\leq 0.1$</td>
</tr>
<tr>
<td>$R_{LOAD}$</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>$V_{ICM,max} - V_{ICM,min}$</td>
<td>$\geq 0.5$ V</td>
</tr>
<tr>
<td>$V_{ID}$</td>
<td>0 V</td>
</tr>
<tr>
<td>$V_{out,pp}$</td>
<td>$\geq 0.6$ V</td>
</tr>
<tr>
<td>$V_{DSat}$</td>
<td>$\geq 100$ mV</td>
</tr>
<tr>
<td>$P_{supply}$</td>
<td>$\leq 2.5$ mW</td>
</tr>
<tr>
<td>Area</td>
<td>minimize</td>
</tr>
</tbody>
</table>

You are free to choose the midpoint of the common mode input range.
The requirement of $V_{ID} = 0$ V means that there should be no differential mode offset: for a 0 V differential input and a common mode input at the midpoint of the common mode input range, the output should be 0 V under nominal supply conditions.

Your circuit should only use the positive $+V_{DD}/2$ and the negative $-V_{DD}/2$ supply.

The design specifications should be met under a variation of the supply voltages of 10% (higher or lower than the nominal voltage). The change in $A_{dm}$ due to the variation in supply voltage should not be more than 1% of its nominal value.

The available components are: NMOS transistors, PMOS transistors and resistors. Ideal sources can only be used to generate the supply voltages, not to generate bias currents.

Area Calculation

Calculate the area by adding up the gate area ($W*L$) of all the transistors and the area of the resistors. For the transistors, the minimum L is 0.13 µm and the minimum W is 0.25 µm. For the resistors, the minimum W and L are 0.5 µm; the sheet resistance is 250 Ω/square.

You are allowed to tie the bulk of any transistor to the source instead of to the positive or negative supply, but at the cost of an area penalty. If you choose to tie the bulk to the source, the area of the transistor should be doubled.

Device Models

```
.model nmos
+ nmos level=1 tox=2.6n vt0=0.3 gamma=0.2 phi=0.6 u0=250 ld=0.025u
+ capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjjg=8e-11
+ lambda=0.2
.model pmos
+ pmos level=1 tox=2.6n vt0=-0.3 gamma=0.2 phi=0.6 u0=100 ld=0.025u
+ capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjjg=8e-11
+ lambda=0.15
```

Grading

100 points total:
   20 points for conciseness and clarity of the report
   20 points for meeting the specifications for everything but $A_{dm}$
   20 points for meeting the $A_{dm}$ specification
   20 points for how well the area is minimized
   20 points for originality of the design