When using the above models, remember to use $W/Leff$ in your calculations, where $Leff=L-2*Ld$ and $Ld=0.025\mu m$. You can calculate $k'$ directly from the SPICE model parameters $u0$ and $tox$.

1. For the circuit shown below, assume $V_{DD}=1.2V$, $W=4\mu m$, $L=0.13\mu m$, $R_D=1K\Omega$, $I_B=600\mu A$.
   a) Calculate $G_{m,dm}$, $G_{m,cm}$, $A_{dm}$ and $A_{cm}$ for $V_{id}=0$ and $V_{ic}=0.8V$, assuming that all the transistors are in saturation.
   b) Verify using SPICE. (To verify using SPICE, use a .tf analysis.)
2. High-swing cascode circuit

The circuit shown below is a high-swing cascode circuit. Assume all the transistors have the same channel length which is 1um and channel width of M1-M4 and M6 is 10um. $I_{\text{ref}}$ and $V_{\text{dsat}}$ of M1 are known. Ignore the channel length modulation and body effect.

a) What is the operation region of M5?

b) If $V_{\text{ds5}} = V_{\text{dsat}}$ of M1. What is the minimum voltage swing at output node such that M1 and M2 are both in saturation? (In terms of $V_{\text{dsat}}$ of M1)

c) If $V_{\text{ds5}} = V_{\text{dsat}}$ of M1. What is the channel width of M5?

3. Self-biased cascode circuit

In the circuit cascode circuit shown on the next page, the resistor R sustains proper voltage to allow both M1 and M2 remain in saturation. Assume both M1 and M2 have the same size W/L. Mobility $\mu_p$ and gate oxide capacitance $C_{\text{ox}}$ are known, ignore the channel length modulation and body effect. What are the minimum and maximum values of $I_{\text{ref}}$ such that M1 and M2 remain in saturation?