1. Assume \((W/L)_{1,2}=50\mu m/0.5\mu m\), \(R_1=1\ k\Omega\), \(R_2=10\ k\Omega\), \(V_{DD}=3\ V\), and the dc level of \(V_{in}\) and \(V_{out}\) are equal. (use the device data shown in Table 2.1, Razavi, p. 37)

(a) Calculate the voltage gain and the output impedance of each circuit.

(b) Calculate the sensitivity of each circuit’s output with respect to the supply voltage. That is, calculate the small-signal “gain” from \(V_{DD}\) to \(V_{out}\).

(c) Verify (a)-(b) with HSPICE using the .TF analysis option.

2. Razavi, problem 3.21 (page 98.)

3. In the below circuit, use \(V_{DD}=1.8\ V\), \(I_{SS}=14\ \mu A\), \(R_D=100\ k\Omega\), \(W=10\ \mu m\), \(L=1\ \mu m\). The device models are given at the end of the assignment.
(a) Calculate $V_{DS}$ of the two transistors by hand, with $V_{ic}=0.9\ V$, $V_{id}=0\ V$, and verify with HSPICE.

(b) Plot $V_{o1}=(V_{o1}-V_{o2})$ vs. $V_{id}$, with $V_{ic}=0.9\ V$ over the range $-1.8 < V_{id} < +1.8\ V$.

(c) Plot $V_{oc}=(V_{o1}+V_{o2})/2$ vs. $V_{ic}$, with $V_{id}=0\ V$ over the range $0 < V_{ic} < +1.8\ V$.

Use SPICE to get these plots. If there are any breakpoints in these plots, explain what causes them and calculate their positions by hand.

(d) Calculate $A_{dm}$ with $V_{ic}=0.9\ V$, $V_{id}=0\ V$. Over what range of $V_{id}$ will the gain remain high? Why does the gain drop off?

(e) Calculate $A_{cm}$ with $V_{ic}=0.9\ V$, $V_{id}=0\ V$.

(f) Calculate $R_{od}$ with $V_{ic}=0.9\ V$, $V_{id}=0\ V$.

Verify (d)-(f) with HSPICE using the .TF analysis option.

4. Repeat problem 3 but replace the $I_{SS}$ current source with a resistor which results in the same $I_{DS}$ currents when $V_{ic}=0.9\ V$ and $V_{id}=0\ V$.

Use the following NMOS and PMOS transistor models for Problem 3 and 4.

```
.model nch nmos LEVEL=1 TOX=2.5n VTO=0.5 KP=140.0e-6 LAMBDA=0.1 +GAMMA=0.5 PHI=0.6
.model pch pmos LEVEL=1 TOX=2.5n VTO=-0.5 KP=65.0e-6 LAMBDA=0.15 +GAMMA=0.5 PHI=0.6
```