1. Design Specification

You are asked to design an operational amplifier used in switched capacitor circuit, shown in Figure 1. Notice that the amplifier is labeled Gm: it is actually an operational trans-conductance amplifier (OTA), since it does not drive a resistive load, but a capacitive load. The practical implication is that there is no need for an output stage with a low output resistance (which is why the sharp end in the amplifier symbol is missing in Figure 1).

The available circuit components are NMOS transistors, PMOS transistors or resistors. Ideal sources can only be used to generate the supply voltages, not to generate bias currents or voltages. The design specifications are as following,

- $L_{\text{min}} = 0.13\,\mu\text{m}$, $W_{\text{min,nmos}} = 0.15\,\mu\text{m}$, $W_{\text{min,pmos}} = 0.15\,\mu\text{m}$, $W$ and $L$ has to be integer multiple of 0.01$\mu\text{m}$.
- Nominal $V_{\text{dd}} = 0.6\,\text{V}$, $V_{\text{ss}} = -0.6\,\text{V}$;
- $C_L = C_F = 250\,\text{fF}$, $C_S = 500\,\text{fF}$;
- $V_{\text{in}}$ peak-peak voltage swings $0.45\,\text{V}$. You are free to choose input common-mode voltage;
- You can apply input offset voltage ($<1\text{mV}$) within your circuit.
- (5pts) settling accuracy is 0.1% with settling time $\leq 20\,\text{ns}$ over $\pm 5\%$ power supply;
- (15pts) $A_{\text{dm}}$: Total differential mode gain $V_{\text{out}}/V_{\text{in}} \geq 6,000$, over the entire output swing range $+0.45\,\text{V}$ to $-0.45\,\text{V}$, and $\pm 5\%$ power supply;
- (10pts) $A_{\text{cm}}$: Total common mode gain $V_{\text{out}}/V_{\text{ic}} \leq 0.1$;
- (10pts) Area $< 1,000\,\mu\text{m}^2$;

The design goal is to
- (10pts) Minimize settling time (nsec)
- (5pts) Minimize the power consumption ($\text{Watts}$) @ nominal $V_{\text{dd}}$ and $V_{\text{ss}}$.  

The closed loop gain of the circuit is (very close to) $C_s/C_F = 2$. Thus, for a 0.45 V peak-to-peak input voltage range, the peak-to-peak output voltage range should be 0.9 V. You are allowed to add an input offset voltage to set your nominal DC output voltage at middle rail (0 V). The amplifier should be able to handle the range of common mode signals resulting from the 0.45 V signal at the input of the overall circuit. You are free to choose the common mode reference VIC. The settling is measured for a step at the input going from 0 to $\pm V_{in,pp}/2$. The settling accuracy of 0.1% includes both dynamic and static settling error.

2. Area Calculation

Calculate the area by adding up the gate area ($W*L$) of all the transistors and the area of the resistors. For the transistors, the minimum $L$ is 0.13 µm and the minimum $W$ is 0.15 µm. For the resistors, the minimum $W$ and $L$ are 0.5 µm; the sheet resistance is 250Ω/square; the capacitor density is 5 fF/um^2. You are allowed to tie the bulk of any transistor to the source instead of to the positive or negative supply, but at the cost of an area penalty. If you choose to tie the bulk to the source, the area of the transistor should be doubled.

3. Device Models

http://bwrc.eecs.berkeley.edu/classes/ee140/dp/model_ee140.sp
The device models are encapsulated in a sub-circuit; use:

x1 d g s b nmos w=10u l=0.13u
x2 d g s b pmos w=10u l=0.13u

to instantiate an NMOS and a PMOS transistor respectively (you have to use the prefix ‘x’ instead of ‘m’). The reason for using a subcircuit is to allow $\lambda$ to decrease with increasing transistor length. The output resistance parameter $\lambda$ will stay the same as before for minimum length transistors ($L_{min}=0.13\mu m$), but will decrease with increasing $L$ (drawn $L$, not effective $L$). Since the output resistance is proportional to $1/\lambda$, the output resistance increases with increasing $L$. Since we are using level-2 device model, it is
worthwhile to calculate level-1 parameters of the device model for your hand calculations. (Ref: problem 1 of HW1, extracting K’, λ, γ, etc.)

A transistor characterization tool, called ‘tchar’, is kindly provided by Ian O’Donnell. You can run from your UNIX account: ‘perl /home/ff/ee140/tchar/tchar140.pl’ For this design problem, only look at the model with proc. TT and temp. 25.

4. Run testbench

Perform dc operation point, AC, and small-signal transfer function analysis:

Testbench 1:
1. Closed loop, transient response, for step input 0 to Vstep, and 0 to -Vstep.
   • Purpose: check specs for tsettle within settling accuracy
2. Vary the power supply by +/- 5%, and re-simulate.

Testbench 2:
1. Closed loop, frequency response.
   • Purpose: check closed loop gain, and 3dB bandwidth to help your design.

Testbench 3:
1. Open loop, differential-mode frequency response with and without loading.
   • Purpose: check Adm, unity gain bandwidth and phase margin to help your design.
2. DC sweeps over entire output swing range.
   • Purpose: check if Adm meets the spec over output swing.
3. Vary the power supply by +/- 5% and re-simulate.

Testbench 4:
1. Open loop, common-mode frequency response with and without loading.
   • Purpose: check if Acm meets the spec.
2. Vary the power supply by +/- 5% and re-simulate.

Usage: put testbench{1-4}_dp4.sp, model_ee140.sp, circuit.sp, parameters.sp in the same directory and run ‘hspice testbench*_dp4.sp -o testbench*_dp4’. There is also circuit_demo.sp (ideal OTA) for you to play with.

5. What to include in your report

http://bwrc.eecs.berkeley.edu/classes/ee140/dp/guidelines_dp4.pdf

6. Grading

100 points total:
45 points for conciseness and clearness of the report
40 points for meeting the specifications
15 points for how well you optimize the goals