Charge sharing

\[ V_{DD} = 2.5 \text{ V} \]

\[ C_{DB} = C_{SB} = 1 \text{ fF} \]

\[ V_{tp} = -0.7 \text{ V} \]

\[ V_{tn} = 0.7 \text{ V} \]

minimum size

\[ w_p = 2w_n \]

\[ C_{IN} = 3 \text{ fF} \]

\[ C_X = 2C_{DB} + C_{IN} = 5 \text{ fF} \]

\[ C_Y = 3C_{DB} + C_{SB} = 4 \text{ fF} \]

1. Is charge sharing a potential problem for this dynamic gate? If so, how can it occur?

2. What is the worst case high voltage at node X? Worst case low?

3. Give 3 ways to fix this.
but maybe not enough, Reservoir caps helps,

\[ V_x = \frac{V_{dd}}{4} \wedge \phi \]

\[ C_x = 4 \, \text{ff} \]

\[ C_y = 4 \, \text{ff} \]

Possible fix: \( \wedge \)
Possible fix #2

Increase size of precharge NMOS to reduce $V_x$ by increasing $C_x$
Still may not be enough + adds cap, thus slowing the evaluate down and increasing power consumption

Possible fix #3
Add a level restorer

* Note: need an NMOS pull-down in this case because we want to restore the level to $\phi$

Possible fix #4
Pre-discharge the internal node, as shown on first page.