1 Complementary CMOS Logic Gate

The figure above is a logic gate we would like to implement using complementary CMOS. The gate is already half-implemented—as you can see, the PMOS pull-up network is already in place but the dotted box below it is not defined yet.

1A What is the logic function of this gate? (F = ???)
1B Using the methods described in the text in the lecture notes, draw the Euler path diagram for both PMOS and NMOS networks.
1C Using your Euler path diagram as a guide, draw the transistor schematic for the NMOS network.
2 Pass-Transmission Gates and Dynamic Logic

The figure below is a logic gate that also incorporates a transmission gate in between the output node F and input node B.

2A Determine the logic function of this gate. (F = ???)

2B We would like to implement this gate using dynamic logic. Give two implementations that yield the same functional output. You may assume that complementary inputs are available.

→ The first implementation using a PMOS pull-up network
→ The second implementation using an NMOS pull-down network
3 Charge sharing

This is a stripped down version of a normally difficult charge sharing analysis problem. Use the figure below and the parameters to calculate the final voltage at node F. Be sure to consider all possible cases.

Supply Voltage = 2.5V  
B, C, D = 0 at all times; F is precharged to Vdd.  
During evaluate cycle, A switches from low to high.  
All transistors are the same size.  $|V_T| = 0.5V$  
Neglect body effect. ☺  
$C_{sb} = C_{db} = 3fF$; Ignore all other caps.  
Also assume that F has a 30fF load attached to it.

4 Dynamic Power Consumption

A simple combinational logic network is shown below.

You may assume that the supply voltage is 2.5V, and that inputs A and B are equally probable to be 0 or 1.

3A Calculate the activity factor for the output of the network shown above. (Node F)

3B Calculate the dynamic power consumption if the inputs are switching at a rate of 150MHz.