EECS 141 – F00
Lecture 13
Homework 6 will be handed out on Th
Software Lab 4 this week
  » Circuit extraction
Midterm 1 grades available next Tu
Project launch on Th!
Important Observation: Noise Margin, Performance, and Power depend upon the applied signals.

- Identify the worst-case for noise margin and performance
- Identify the average case for average power and energy
- Identify the worst-case for peak-power
Today’s Lecture

- Power dissipation (continued)
- Alternative logic styles – static
  » Ratioed logic
  » Pass-transistor logic
Low Power Design

The contributions of A. Chandrakasan, T. Sakurai, and Kuroda are greatly appreciated.
Factors Affecting Transition Activity, $\alpha_{0->1}$

- “Static” component (does not account for timing)
  - Type of Logic Function (NOR vs. XOR)
  - Type of Logic Style (Static vs. Dynamic)
  - Signal Statistics
  - Inter-signal Correlations

- “Dynamic” or timing dependent component
  - Circuit Topology
  - Signal Statistics and Correlations
Transition Probabilities

\[ P_{0\to1}(\text{NOR, NAND}) = \frac{2^N - 1}{2^N} \quad P_{0\to1}(\text{XOR}) = \frac{1}{4} \]
Inter-signal Correlations

(a) Logic circuit without reconvergent fanout

(b) Logic circuit with reconvergent fanout

\[ p_{0\rightarrow 1} = (1 - p_a p_b) p_a p_b = \frac{3}{16} \]

\[ p_z = p(C=1|B=1) \cdot p(B=1) \]

\[ p_{0\rightarrow 1} = 0 \]

- Need to use conditional probabilities to model inter-signal correlations!
- CAD tools required for such analysis
Taking Delay into Account: Glitching or “Dynamic Hazards”

May cause $\alpha_{01} > 1$
Example: Adder Circuit

- Diagram showing a series of adder circuits labeled Add0 to Add15.
- Each adder circuit has inputs and outputs labeled S0, S1, S2, and S14, S15.
- The input for the first adder is labeled Cin.
- A graph shows the sum output voltage over time, with time in nanoseconds on the x-axis and voltage in volts on the y-axis.
- The graph includes curves labeled S1, S5, S10, S14, and S15.
Solution: Balanced delay paths

Ripple

Lookahead
Principles for Power Reduction

● Prime choice: Reduce voltage!
  » Recent years have seen an acceleration in supply voltage reduction
  » Design at very low voltages still open question (0.6 ... 0.9 V by 2010!)

● Reduce switching activity

● Reduce physical capacitance
Review: EDP Plot

![Graph showing Energy-Delay, Energy, and Delay as functions of V_DD (V).]
Ratioed Logic

(a) Resistive load
(b) Depletion load NMOS
(c) PMOS load

Goal: to reduce the number of devices over complementary CMOS
Ratioed Logic

- N transistors + Load
- \( V_{OH} = V_{DD} \)
- \( V_{OL} = \frac{R_{PN}}{R_{PN} + R_L} \)
- Assymetrical response
- Static power consumption
- \( t_{pL} = 0.69 R_L C_L \)
Active Loads

Depletion Load

PMOS Load

depletion load NMOS

pseudo-NMOS
Load Lines of Ratioed Gates

![Graph showing load lines for different types of loads: Current source, Pseudo-NMOS, Depletion load, and Resistive load. The graph plots $I_L$ (Normalized) against $V_{out}$ (V).]
Pseudo-NMOS

\[ V_{OH} = V_{DD} \text{ (similar to complementary CMOS)} \]

\[ k_n \left( (V_{DD} - V_{Tn}) V_{OL} - \frac{V_{OL}^2}{2} \right) = \frac{k_p}{2} (V_{DD} - |V_{Tp}|)^2 \]

\[ V_{OL} = (V_{DD} - V_T) \left[ 1 - \sqrt{1 - \frac{k_p}{k_n}} \right] \text{ (assuming that } V_T = V_{Tn} = |V_{Tp}|) \]

*SMALLER AREA & LOAD BUT STATIC POWER DISSIPATION!!!
Pseudo-NMOS NAND Gate

\[ C_{L,\text{pseudo}} = 0.5 \, C_{L,\text{CMOS}} \, \text{(Fan-out of 1)} \]
Improved Loads

Adaptive Load
Improved Loads (2)

Dual Cascode Voltage Switch Logic (DCVSL)
Example

XOR-NXOR gate
Pass-Transistor Logic

- N transistors
- No static consumption
NMOS-only switch

$V_B$ does not pull up to 5V, but $5V - V_{TN}$

Threshold voltage loss causes static power consumption
Solution 1: Transmission Gate

\[ A = 5 \text{ V}, \quad C = 5 \text{ V}, \quad C = 0 \text{ V} \]
Resistance of Transmission Gate

(W/L)_p = (W/L)_n = 1.8/1.2

![Graph showing the resistance of transmission gate with labels R_p, R_n, and R_eq against Vout.]
Pass-Transistor Based Multiplexer
Transmission Gate XOR
Delay in Transmission Gate Networks

(a)

(b)

(c)
Delay Optimization

• Delay of RC chain

\[ t_p = 0.69 \sum_{k=0}^{n} CR_{eq}^k = 0.69 CR_{eq} \frac{n(n+1)}{2} \]

• Delay of Buffered Chain

\[ t_p = 0.69 \left[ \frac{n}{m} CR_{eq} \frac{m(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right) t_{buf} \]

\[ = 0.69 \left[ CR_{eq} \frac{n(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right) t_{buf} \]

\[ m_{opt} = 1.7 \sqrt{\frac{t_{pbuf}}{CR_{eq}}} \]
Transmission Gate Full Adder

Sum Generation

Carry Generation

Setup
(2) NMOS Only Logic: Level Restoring Transistor

- Advantage: Full Swing
- Disadvantage: More Complex, Larger Capacitance
- Other approaches: reduced threshold NMOS
Level Restoring Transistor

(a) Output node

(b) Intermediate node X
Solution 3: Single Transistor Pass Gate with $V_T=0$

WATCH OUT FOR LEAKAGE CURRENTS
Complimentary Pass Transistor Logic

(a)

Pass-Transistor Network

Inverse Pass-Transistor Network

(b)

AND/NAND

OR/NOR

EXOR/NEXOR

F = A \oplus B

F = A + B

F = A \odot B \bar{Y}

\begin{align*}
\text{F} &= \overline{A} \otimes B \\
\text{F} &= A \oplus B \\
\text{F} &= A + B
\end{align*}