Administrivia

- Homework 6 will be handed out on Th
- Software Lab 4 this week
  - Circuit extraction
- Midterm 1 grades available next Tu
- Project launch on Th!
Last Lecture

- Power dissipation (continued)
- Alternative logic styles – static
  » Ratioed logic

  Trades off noise margin and power for performance and area
Today’s Lecture

- Project Launch
- Combinational Logic - STATIC
  - Ratioed Logic
  - Pass-transistor Logic
PROJECT
A 512x64 CAM Memory

- Control Logic
- R/W Address (9 bits)
- Data (64 bits)
- Comparand
- Mask
- CAM Array
- Address Decoder
- Priority Encoder
- 2^n Validity Bits
- I/O Buffers
- Commands
Example: CAM with 6 entries

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0x674243A4</td>
</tr>
<tr>
<td>1</td>
<td>0x6725643E</td>
</tr>
<tr>
<td>2</td>
<td>0x68425786</td>
</tr>
<tr>
<td>3</td>
<td>0x12D64368</td>
</tr>
<tr>
<td>4</td>
<td>0xE4B64802</td>
</tr>
<tr>
<td>5</td>
<td>0x75367843</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Comparand</th>
<th>Mask</th>
<th>Match?</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x674243A4</td>
<td>0xFFFFFFFF</td>
<td>Y</td>
<td>0</td>
</tr>
<tr>
<td>0x89424858</td>
<td>0x00FF0000</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>0x05943864</td>
<td>0x0000F000</td>
<td>N</td>
<td>N/A</td>
</tr>
<tr>
<td>0x3859AB34</td>
<td>0x00000000</td>
<td>Y</td>
<td>5</td>
</tr>
</tbody>
</table>
Phase 1: The Priority Encoder

vm[0] → match
vm[1] → em[0]
... → ...
vm[511] → em[8]
Project Goals and Constraints

- Choose between three different goals
  - Minimize area (40 nsec max delay)
  - Minimize delay
  - Minimize average energy (40 nsec max delay)
- Freedom in implementation choices
  - Static or dynamic
- Some constraints
  - 2.5 V max (no minimum)
  - 0.25 micron CMOS
The importance of the project report

- Limit of 3 pages to convince us that your project should get a Nobel prize (or at least a major award)
- Be concise and to the point
- Demonstrate clearly that your claims are true
- Express your motivations and your reasoning. Make sure to make it quantitative
- Be honest – we will check your spice files and run them!
Recommended Reading

- Chapter 6 (new version)
- Chapter 10 (old version) – study the decoder section
- Chapter 7 (old version)
- Weste and Eshragian
Other recommendations

- Do not start with “optimization by simulation”
- Think through the problem first and build a first-order analytical model to start
- DO NOT FORGET WIRING
Improved Loads

Adaptive Load
Improved Loads (2)

Dual Cascode Voltage Switch Logic (DCVSL)
Example

XOR-NXOR gate
Pass-Transistor Logic

- N transistors
- No static consumption
NMOS-only switch

\[ V_B \text{ does not pull up to 5V, but } 5V - V_{TN} \]

Threshold voltage loss causes static power consumption
Solution 1: Transmission Gate
Resistance of Transmission Gate

(W/L)_p = (W/L)_n = 1.8/1.2
Pass-Transistor Based Multiplexer
Transmission Gate XOR
Delay in Transmission Gate Networks

(a)

(b)

(c)
Delay Optimization

• Delay of RC chain

\[ t_p = 0.69 \sum_{k=0}^{n} CR_{eq} k = 0.69 CR_{eq} \frac{n(n+1)}{2} \]

• Delay of Buffered Chain

\[ t_p = 0.69 \left( \frac{n}{m} CR_{eq} \frac{m(m+1)}{2} \right) + \left( \frac{n}{m} - 1 \right) t_{buf} \]

\[ = 0.69 \left[ CR_{eq} \frac{n(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right) t_{buf} \]

\[ m_{opt} = 1.7 \sqrt{\frac{t_{buf}}{CR_{eq}}} \]
Transmission Gate Full Adder

Sum Generation

Carry Generation

Setup
(2) NMOS Only Logic: Level Restoring Transistor

- Advantage: Full Swing
- Disadvantage: More Complex, Larger Capacitance
- Other approaches: reduced threshold NMOS
Level Restoring Transistor

(a) Output node

(b) Intermediate node X
Solution 3: Single Transistor Pass Gate with $V_T=0$

WATCH OUT FOR LEAKAGE CURRENTS
Complimentary Pass Transistor Logic

(a)

(b)

AND/NAND

OR/NOR

EXOR/NEXOR
4 Input NAND in CPL