Lecture 24

Dealing with Interconnect
Administrivia

- Project phase 2 extended till Th 5pm.
  » Halt all efforts and work on your report!
- No regrades of Midterm 2 after next Tu.
Today’s Lecture

- Dealing with capacitive interconnect
- Dealing with resistive interconnect
COPING WITH INTERCONNECT
Impact of Interconnect Parasitics

- Reduce Reliability
- Affect Performance

Classes of Parasitics
- Capacitive
- Resistive
- Inductive
Dealing with Capacitance
Capacitive Crosstalk
Dynamic Node

3 x 1 μm overlap: 0.19 V disturbance
Capacitive Crosstalk Driven Node

\[ \tau_{XY} = R_Y (C_{XY} + C_Y) \]

Keep time-constant smaller than rise time
Delay Degradation

- Impact of neighboring signal activity on switching delay
- When neighboring lines switch in opposite direction of victim line, delay increases

Miller Effect

- Both terminals of capacitor are switched in opposite directions
  \((0 \rightarrow V_{dd}, \ V_{dd} \rightarrow 0)\)
- Effective voltage is doubled and additional charge is needed
  \((\text{from } Q=CV)\)
Interconnect Projections
Low-k dielectrics

- Both *delay and power are reduced* by dropping interconnect capacitance
- Types of low-k materials include: inorganic (SiO$_2$), organic (Polyimides) and aerogels (ultra low-k)
- The numbers below are on the conservative side of the NRTS roadmap

<table>
<thead>
<tr>
<th>Generation</th>
<th>0.25 µm</th>
<th>0.18 µm</th>
<th>0.13 µm</th>
<th>0.1 µm</th>
<th>0.07 µm</th>
<th>0.05 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Constant</td>
<td>3.3</td>
<td>2.7</td>
<td>2.3</td>
<td>2.0</td>
<td>1.8</td>
<td>1.5</td>
</tr>
</tbody>
</table>
How to Battle Capacitive Crosstalk

- Avoid large crosstalk cap’s
- Avoid floating nodes
- Isolate sensitive nodes
- Control rise/fall times
- Shield!
- Differential signalling
Structured and Predictable Interconnect

Example: Dense Wire Fabric (DWF) [Khatri, DAC99]

Trade-off:
• Cross-coupling capacitance 40x lower, 2% delay variation
• Increase in area and overall capacitance
Driving Large Capacitances

\[ t_{pHL} = \frac{C_L \cdot V_{swing}}{2} \]

Transistor Sizing
Using Cascaded Buffers

\[ u_{opt} = e \]
$t_p$ in function of $u$ and $x$
Impact of Cascading Buffers

<table>
<thead>
<tr>
<th>$x$</th>
<th>Unbuffered</th>
<th>Single Buffer</th>
<th>Cascaded Buffers</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>10</td>
<td>6.3</td>
<td>6.3</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
<td>20</td>
<td>12.5</td>
</tr>
<tr>
<td>1000</td>
<td>1000</td>
<td>63</td>
<td>18.8</td>
</tr>
<tr>
<td>10,000</td>
<td>10,000</td>
<td>200</td>
<td>25.0</td>
</tr>
</tbody>
</table>

$t_{opt}/t_{p0}$ versus $x$ for various driver configurations.

$C_{in} = 10 \text{ fF in 1 \mu m CMOS}$
Output Driver Design

Driver for 20 pF Load

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_n$ (µm)</td>
<td>1.8</td>
<td>5.3</td>
<td>15.8</td>
<td>47.7</td>
<td>138.2</td>
<td>409.0</td>
<td>1210.7</td>
</tr>
<tr>
<td>$W_p$ (µm)</td>
<td>2.8</td>
<td>8.4</td>
<td>24.9</td>
<td>73.8</td>
<td>218.3</td>
<td>646.2</td>
<td>1912.8</td>
</tr>
</tbody>
</table>

Transistor sizes for optimally sized cascaded buffers.

$t_p = 4.2$ ns

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_n$ (µm)</td>
<td>1.8</td>
<td>22.7</td>
<td>286.0</td>
</tr>
<tr>
<td>$W_p$ (µm)</td>
<td>2.8</td>
<td>35.3</td>
<td>444.5</td>
</tr>
</tbody>
</table>

Transistor Sizes of Optimized Cascaded Buffer.

$t_p = 7.6$ ns
How to Design Large Transistors

(a) small transistors in parallel

(b) circular transistors
Bonding Pad Design

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Reducing the swing

\[ t_{pHL} = \frac{C \cdot V_{swing}}{I_{av}} \]

- Reducing the swing potentially yields linear reduction in delay
- Also results in reduction in power dissipation
- Requires use of “sense amplifier” to restore signal level
Charge Redistribution Amplifier

![Charge Redistribution Amplifier Diagram]

(a) Diagram of the charge redistribution amplifier with transistors M1, M2, and M3, and capacitors C_A and C_B.

Graph showing the time-domain behavior of the amplifier:
- Time axis (x-axis): 0.0 to 3.00 nsec
- Voltage axis (y-axis): 0.0 to 5.00

- V_ref = 3V
- V_B as a function of time
- V_A as a function of time
- V_in as a function of time

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Precharged Bus
Tristate Buffers
Dealing with Resistance
RI Introduced Noise

\[ V_{DD} - \Delta V' \]

\[ \phi_{pre} \]

\[ I \]

\[ R' \]

\[ X \]

\[ \Delta V \]
Power and Ground Distribution

(a) Finger-shaped network  
(b) Network with multiple supply pins
Resistance and the Power Distribution Problem

- Requires fast and accurate peak current prediction
- Heavily influenced by packaging technology

Source: Simplex
Limit the dc-current to 1 mA/μm.
Electromigration (2)
The Impact of Resistivity

Diffused signal propagation

Delay $\sim L^2$
The Global Wire Problem

\[ T_d = 0.377 R_w C_w + 0.693 (R_d C_{out} + R_d C_w + R_w C_{out}) \]

Challenges

- No further improvements to be expected after the introduction of Copper (superconducting, optical?)

- Design solutions
  - Use of fat wires
  - Insert repeaters — but might become prohibitive (power, area)
  - Efficient chip floorplanning

- Towards “communication-based” design
  - How to deal with latency?
  - Is synchronicity an absolute necessity?
Reducing RC-delay

Repeater

\[ M = L \frac{0.38rc}{\sqrt{t_{pbuf}}} \]
Architecture Must Evolve to Fit the Landscape

Global operations
Low bandwidth
High latency &
High power

Local, parallel operations
High bandwidth
Low latency &
Low power

Source: Bill Dally, Stanford
Interconnect:

# of Wiring Layers

# of metal layers is steadily increasing due to:

- Increasing die size and device count: we need more wires and longer wires to connect everything
- Rising need for a hierarchical wiring network; local wires with high density and global wires with low RC

0.25 µm wiring stack

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Interconnect Projections: Copper

- Copper is planned in full sub-0.25 µm process flows and large-scale designs (IBM, Motorola, IEDM97)
- With cladding and other effects, Cu ~ 2.2 µΩ-cm vs. 3.5 for Al(Cu) ⇒ 40% reduction in resistance
- Electromigration improvement; 100X longer lifetime (IBM, IEDM97)
  » Electromigration is a limiting factor beyond 0.18 µm if Al is used (HP, IEDM95)

Vias