Physical Layout of ACS Unit

In the second phase of the project, you are to realize a physical design of the ACS Unit designed in Phase I. The design should be laid out using the tool of your choice. The supported tool is ‘Electric’, which is available for download off the web site.

As with any layout assignment, you will quickly discover that drawing layout is much simpler if you plan things out ahead of time. It is much easier to have a general layout strategy than to just blindly draw objects on the screen. For example, it is important to plan out how to distribute the supply and ground rails in your design. In addition, a design that is very regular can easily be tiled and reused, saving you a lot of time.

Use common sense in laying out your circuit and remember that long transistors must be built properly. Consult your textbook if you don’t have a clue how to do this!

Updating of Results

Most probably, mapping your design into a physical implementation will probably cause some important changes in the energy and delay numbers. In addition, you must ensure that your layout and schematic are functionally equivalent (this is called Layout-Versus-Schematic or LVS). Hence, it is essential that you perform a full functional and performance analysis on the extracted circuit schematics.

The goal of this phase of the project is to compare the results before and after physical design, not to improve on the design goals. Explain any major deviations from your results in Phase I. Try not to make any significant changes to your original design of Phase I. You may make minor modifications to the circuit that do not change the underlying principles that govern the circuit behavior of the design. If you find it necessary to alter a major part of your circuit (because of non-functionality or unacceptable results), a full motivation should be provided in the report.

Also, changes in the design goal are NOT allowed!

Report

Your report for this phase of the project serves to accomplish two things:

1) You should discuss your overall layout strategy and how it is related to your original design goals.

2) Compare your results in this phase to those that you obtained in the first phase of the project, including any changes you made to the design.
The total report should not contain more than **two** pages of text. You may attach additional pages for figures, but DO NOT PRINT OUT THE LAYOUTS FOR ALL THE CELLS. Use the following guidelines to govern your report content and length:

→ Page 1: Executive summary, overall design decisions, remarks, and motivations.
→ Page 2: Layout strategy for a single stage in the design, analysis of simulation results, and comparison to phase 1

In addition to the report, you must electronically submit the extracted SPICE input deck used to obtain the energy analysis to msheets@eecs.berkeley.edu. Remember, the quality of the report is major factor in deciding your final project grade for this phase.

**Grading Scheme**

Phase 2 is worth 40% of the total grade on the project. (Phase 1 is worth 60%). Your Phase 2 grade is divided evenly between your general approach and correctness (50%), and the quality of your report (50%).

**Frequently Asked Questions**

Q: Electric has an automatic layout generator. Can we use that?
A: It is not recommended. You should design the cell and its constituent sub-cells completely by hand. You will often find that automatic layout generators do lousy jobs. I’ll be very surprised if you get anything working with that.

Q: Our design in Phase 1 was pretty fast, so I was wondering if I could switch from Power optimization to Speed optimization.
A: No. You must stick with your original design goals. No exceptions.

Q: How can I fit a printout of all my cells into two pages?
A: I do not care to examine each of your cells. Just print the main cell as large as you have room for it on the page. I really just want to see that your design is regular or has some structure. The “greatness” of the design can be verified by examining your explanation as well as delay, power, and area data.