Link Your SPICE Model Correctly

.lib '/home/aa/grad/huifangq/g25b.mod' TT

- You'll notice that there are four corners, TT, FF, SS, FS, SF. These represent the different variation extremes we can expect due to process variations. For example, TT stands for NMOS: typical, PMOS: typical. FS stands for NMOS: fast, PMOS: slow etc.

- Our homework sets will typically use the TT model.

- For Hw2 problem 4, add the following line in your spice deck, instead of the link to the g25b.mod ahead:

  .MODEL nmos NMOS VTO=0.6 GAMMA=0.5 PHI=0.6 KP=20E-6 LAMBDA=0.05
  .MODEL pmos PMOS VTO=-0.6 GAMMA=0.5 PHI=0.6 KP=7E-6 LAMBDA=0.1

  (Use micron as the unit of W and L for transistors in problem 4!)
Some Issues Related to Lab2

- Good that most people in the lab got through with no problem. Keep on your good job!

- Max is frozen sometime
  - ‘Max &’ doesn’t really execute Max parallel as ‘Emacs &’ does
  - Open a second SSH window for all other operations like copying and checking email. Do not disturb Max when it’s working.

- Some times the layer selection and wire drawing becomes weird in Max. Check to see if there’s some layers disabled there — the layer name turns dark after you click on it, which means that it’s disabled.

Typical Assumptions in Problem Set

- In digital design problems, if not specified otherwise, you can assume the following:
  - Bulk of PMOS is connected to Vdd, while bulk of NMOS is grounded.
  - When $V_{SB}$ of a device is not 0, you’ll need to take the body effect on Vth into consideration during circuit analysis.
  - The object of study is short channel device when the Vdsat data is given.
  - You can always use .MODEL command to simulate your circuits with certain process parameters, without sticking to the g25.mod model.
Typical Problems in Hw2
— Digital Vs. Analog

• It’s interesting to view some digital problems from an analog perspective.
  – The small signal model used in analog analysis would help you in understanding the transient behavior of circuits better. E.g. the switching gain of an inverter.
  – It may provide more accurate results than the digital large signal analysis.

• However in this class it may be more important to develop a digital mind set in circuit analysis.
  – Digital focus on different metrics of circuit than analog: the steady state value of $V_{MIN}$, $V_{OH}$, $V_{OL}$; the delay and power.
  – Digital always applies large signal analysis at fixed operation point.
Typical Problems in Hw2
— Saturation Vs. Vel. Saturation

• A long channel device operates in either linear or saturation region (quadratic $I_d$ equation applied).

• A short channel device can operate in either linear, saturation or vel. saturation region. (Fig 3-24 @ Pg. 102)
  – The difference is that both saturation happen when $V_{ds} > \min(V_{gt}, V_{dsat})$,
  – But in saturation $\min(V_{gt}, V_{dsat}) = V_{gt}$,
  – In vel. saturation $\min(V_{gt}, V_{dsat}) = V_{dsat}$.

Typical Problems in Hw2
— Noise Margin Calculation

• Definition on textbook Pg. 21
  \[
  \begin{align*}
  N_{M_H} &= V_{OH} - V_{IH} \\
  N_{M_L} &= V_{IL} - V_{OL}
  \end{align*}
  \]

• However NM calculation is usually simplified in hand analysis:
  – When the switch transition is fast, the gain is approximated to be close to infinite, then $V_{IH} \approx V_M \approx V_{IL}$. This usually happens when the pull-up and pull-down devices are both strong enough.
  – When $V_{OH}$ and $V_{OL}$ are still close to $V_{dd}$ and ground (not too far away), they can be computed assuming $V_{in} = 0$ and $V_{dd}$ respectively. — In the strict sense $V_{OH}$ is the output voltage when $V_{in} = 0$, and $V_{OL}$ is the output voltage when $V_{in} = V_{OH}$.
Typical Problems in Hw2
— Verhmi Voltage

- For NMOS, $2\Phi_F = -0.6v$
- For PMOS, $2\Phi_F = 0.6v$

Safer but Slower!