1 Generating a Voltage Transfer Characteristic

The circuit below features an NMOS transistor that is coupled with a non-linear load device represented by the shaded box. Also shown are the I-V characteristics for the transistor and load device.
1A Draw the VTC for this circuit. Determine (or estimate, if necessary, from your VTC) the following parameters: $V_{OH}$, $V_{OL}$, $V_M$

1B This circuit can be used as an alternative to a traditional CMOS inverter (where the non-linear device is a PMOS transistor). From the concepts discussed thus far in lecture and from the results of your VTC, what are the disadvantages of this method?

2 Analysis Using the Unified Model

Below is another I-V transfer curve for a different NMOS transistor operating under slightly different conditions:

![I-V Transfer Curve](image)

In this problem, the objective is to use a transfer curve like the one above to obtain information about the transistors. The transistor has (W/L)=(1/1). You may also assume that velocity saturation does not play a role in this example. Also assume $-2\Phi_F = -0.6V$

2A From the figure above, determine the following parameters: $V_{TH}$, $\gamma$, $\lambda$.

2B Using SPICE, generate the family of curves for a PMOS transistor with the following parameters. Make sure you add the following library card to your deck. It specifies that we want 0.25 micron MOSFETs with both NMOS and PMOST characterized under Typical conditions.

```
.lib "g25.mod" TT
```

You must also copy the g25.mod file to your working directory:

```
cp ~msheets/pub/ee141/g25.mod .
```
3 Device Parameters Part 2

Below is a table showing a set of measurements performed on a newly fabricated MOS transistor. We need to make a hand analysis model for them. Based upon the fabrication characteristics, we expect that \( V_{DSAT} = -0.8 \) V.

<table>
<thead>
<tr>
<th>Measurement Number</th>
<th>( V_{GS} )</th>
<th>( V_{DS} )</th>
<th>( V_{SB} )</th>
<th>( I_D )</th>
<th>Operation Region</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-2.5V</td>
<td>-2.5V</td>
<td>0</td>
<td>-95.88uA</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1.0V</td>
<td>1.0V</td>
<td>0</td>
<td>0.00 uA</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>-0.7V</td>
<td>-0.7V</td>
<td>0</td>
<td>-2.83 uA</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>-2.0V</td>
<td>-2.5V</td>
<td>0</td>
<td>-67.68 uA</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>-2.5V</td>
<td>-2.5V</td>
<td>-0.8V</td>
<td>-80.65 uA</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>-2.5V</td>
<td>-1.5V</td>
<td>0</td>
<td>-90.17 uA</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>-2.5V</td>
<td>-0.6V</td>
<td>0</td>
<td>-67.52 uA</td>
<td></td>
</tr>
</tbody>
</table>

You may assume that \( V_{DSAT} = -1.0 \) V and \(-2\Phi_F = 0.6 \) V and that the device follows the [UNIFIED MOS MODEL](Figure 3-23, page 102).

3A Is the measured transistor a PMOS or an NMOS device? Explain your answer.

3B From measurements above, determine the following parameters: \( V_T, \gamma, \lambda \).

3C Determine the operating region for each measurement to complete the missing column in the table (LINEAR, CUTOFF, SATURATION, or VEL. SATURATION).
4 RTL Circuit + First Order Delay Analysis

The figure below is a very atypical RTL circuit where the active device is a PMOS transistor. Normally and in the old days, transistors utilizing RTL design styles employed an NMOS transistor with a resistive load.

Because we haven’t yet covered timing analysis using the full transistor model, you may assume the following information about the problem. Assume the switch model behavior of the PMOS transistor. When Vin > 1.25V, the resistance of the transistor is infinite. When Vin < 1.25V, the transistor can be modeled as having a resistance of 100 ohms.

4A Determine the values for $V_{OH}$ and $V_{OL}$. Explain your answer.
4B Calculate $t_{p_{LH}}$ and $t_{p_{HL}}$ to obtain the average propagation delay, $t_p$. 