1 Memory Cells

The 2-T memory cell uses 2 identical transistors with W/L = 0.3/0.2. Separate lines are provided for the read select (RS) and write select (WS), which both switch between 0 and 1.5V. The Bit Line is precharged to Vdd/2 prior to a read. A write is done by pulling the Bit Line either to Vdd or to GND. Ignore body effect and channel-length modulation. ($\gamma=0; \lambda=0$). Use:

\begin{align*}
V_{t_{0,n}} &= 0.4 \text{ V} \\
K' &= 110 \text{ uA/V}^2 \\
V_{DSAT} &= 0.6 \text{ V} \\
|\Phi_F| &= 0.6 \text{ V}
\end{align*}

1A Explain the operation of the memory. Draw waveforms for BL, WS, and RS and Vx for reads and writes of both '1's and '0's.

1B Determine maximum current through transistors during a read operation.

1C The bit line is connected to a single-ended sense amp which would have a switching threshold of 200mV in either direction from Vdd/2. Compute the time required to read a data bit. Assume $C_c=10\text{fF}$ and $C_b=2\text{pF}$. 

![Memory Cell Diagram]
2 DRAM Memory Cell

A single-transistor DRAM cell is represented by the following circuit diagram. The bit line can be precharged to $V_{DD}/2$ by using a clocked precharge circuit. Also the WRITE circuit is assumed here to bring the potential of the bit line to $V_{DD}$ or 0V during the WRITE operation with word line at $V_{DD}$. Using the parameters given:

- $V_{in,n} = 1.0 \text{ V}$
- $\gamma = 0.3 \text{ V}^{1/2}$
- $|2\phi_F| = 0.6\text{V}$

### 2A
Find the maximum voltage across the storage capacitor $C_s$ after WRITE-1 operation, i.e., when the bit line is driven to $V_{DD} = 5\text{V}$.

### 2B
Assuming zero leakage current in the circuit, find the voltage at the bit line during READ-1 operation after the bit line is first precharged to $V_{DD}/2$. 

[Diagram of DRAM cell with labels for Word Line, Precharge circuit, Write Circuit, bit line, $C_{Bl} = 450 \text{fF}$, and $C_s = 50\text{fF}$]