EE141- Spring 2003
Lecture 13
CMOS Logic

Announcements

- Midterms Results
- Project Launch
- Last software lab this week
- New homework on Th
Today’s lecture

- Transmission Lines
- CMOS Logic

The Transmission Line

\[ \frac{2v}{\lambda^2} - r \frac{dv}{dt} + kc^2 \frac{d^2v}{dt^2} = 0 \]

The Wave Equation
Wave Reflection for Different Terminations

Transmission Line Response ($R_L = \infty$)
Lattice Diagram

Critical Line Lengths versus Rise Times

Critical Transmission Line Lengths for Various Rise Times

\[ v = \frac{c_0}{\sqrt{\tau}} = 15 \text{ cm/nsec} \]

<table>
<thead>
<tr>
<th>Rise Time (ps)</th>
<th>Critical Line Length ( l_{\text{crit}} = vt_e/2.5 ) (cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>0.3</td>
</tr>
<tr>
<td>100</td>
<td>0.6</td>
</tr>
<tr>
<td>250</td>
<td>1.5</td>
</tr>
<tr>
<td>500</td>
<td>3.0</td>
</tr>
<tr>
<td>750</td>
<td>4.5</td>
</tr>
<tr>
<td>1000</td>
<td>6.0</td>
</tr>
</tbody>
</table>

\[ L_{\text{crit}} \approx 1\text{ cm} \]

100-200ps today

Typical Rise Times for IC Technologies (1990, Bakoglu)

<table>
<thead>
<tr>
<th>Technology</th>
<th>On-Chip Rise Times</th>
<th>Off-Chip Rise Times</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>0.5–2 nsec</td>
<td>2–4 nsec</td>
</tr>
<tr>
<td>Bipolar</td>
<td>50–200 nsec</td>
<td>200–400 nsec</td>
</tr>
<tr>
<td>GaAs</td>
<td>20–100 nsec</td>
<td>100–250 nsec</td>
</tr>
</tbody>
</table>
Design Rules of Thumb

- Transmission line effects should be considered when the rise or fall time of the input signal \( (t_r, t_f) \) is smaller than the time-of-flight of the transmission line \( (t_{flight}) \):
  \[ t_r (t_f) \ll 2.5 t_{flight} \]
- Transmission line effects should only be considered when the total resistance of the wire is limited:
  \[ R < 5 Z_0 \]
- The transmission line is considered lossless when the total resistance is substantially smaller than the characteristic impedance,
  \[ R < Z_0 / 2 \]

Should we be worried?

- Transmission line effects cause overshooting and non-monotonic behavior

Clock signals in 400 MHz IBM Microprocessor (measured using e-beam prober) [Restle98]
CMOS Logic

Static CMOS
- Conventional Static CMOS Logic
- Ratioed Logic
- Pass Transistor/Transmission Gate Logic

Dynamic CMOS Logic
- Domino
- np-CMOS

Combinational vs. Sequential Logic

(a) Combinational
Output = \( f(In) \)

(b) Sequential
Output = \( f(In, Previous\ In) \)
Static CMOS Circuit

At every point in time (except during the switching transients) each gate output is connected to either \( V_{DD} \) or \( V_{ss} \) via a low-resistive path.

The outputs of the gates assume at all times the value of the Boolean function, implemented by the circuit (ignoring, once again, the transient effects during switching periods).

This is in contrast to the dynamic circuit class, which relies on temporary storage of signal values on the capacitance of high impedance circuit nodes.

Static Complementary CMOS

PUN and PDN are dual logic networks
NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal. NMOS switch closes when switch control input is high.

NMOS Transistors pass a “strong” 0 but a “weak” 1

PMOS Transistors in Series/Parallel Connection

PMOS switch closes when switch control input is low.

PMOS Transistors pass a “strong” 1 but a “weak” 0
Threshold Drops

Complementary CMOS Logic Style Construction

- PUP is the **DUAL** of PDN (can be shown using DeMorgan’s Theorem’s)
  
  \[
  \overline{A + B} = AB \\
  \overline{AB} = \overline{A} + \overline{B}
  \]

- The complementary gate is inverting

\[\text{AND} = \text{NAND} + \text{INV}\]
Example Gate: NAND

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
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Truth Table of a 2 input NAND gate

PDN: $G = AB \Rightarrow$ Conduction to GND

PUN: $F = \overline{A + B} = \overline{AB} \Rightarrow$ Conduction to $V_{DD}$

$G(In_1, In_2, In_3, \ldots) = F(In_1, \overline{In}_2, \overline{In}_3, \ldots)$

Example Gate: NOR

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<thead>
<tr>
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Truth Table of a 2 input NOR gate

OUT = $\overline{A + B}$
Complex CMOS Gate

\[ \text{OUT} = D + A \cdot (B + C) \]

Cell Design

- **Standard Cells**
  - General purpose logic
  - Can be synthesized
  - Same height, varying width

- **Datapath Cells**
  - For regular, structured designs (arithmetic)
  - Includes some wiring in the cell
  - Fixed height and width
Standard Cell Layout Methodology – 1980s

Routing channel
signals

Standard Cell Layout Methodology – 1990s

Mirrored Cell
No Routing channels

M2
M3
Cell height 12 metal tracks
Metal track is approx. $3\lambda + 3\lambda$
Pitch = repetitive distance between objects

Cell height is “12 pitch”

Rails $\sim 10\lambda$

With minimal diffusion routing

With silicided diffusion
Standard Cells

2-input NAND gate

Stick Diagrams

Contains no dimensions
Represents relative positions of transistors

Inverter

NAND2
Stick Diagrams

$$X = C \cdot (A + B)$$

Two Versions of $C \cdot (A + B)$
Consistent Euler Path

\[ X = (A + B)(C + D) \]

OAI22 Logic Graph
Example: \( x = ab+cd \)

(a) Logic graphs for \((ab+cd)\)  
(b) Euler Paths \(\{a\ b\ c\ d\}\)  
(c) stick diagram for ordering \(\{a\ b\ c\ d\}\)

Multi-Fingered Transistors

One finger  
Two fingers (folded)  
Less capacitance
Properties of Complementary CMOS Gates

Snapshot

High noise margins:
$V_{OH}$ and $V_{OL}$ are at $V_{DD}$ and $GND$, respectively.

No static power consumption:
There never exists a direct path between $V_{DD}$ and $V_{SS}$ ($GND$) in steady-state mode.

Comparable rise and fall times:
(under appropriate sizing conditions)

CMOS Properties

- Full rail-to-rail swing; high noise margins
- Logic levels not dependent upon the relative device sizes; ratioless
- Always a path to Vdd or Gnd in steady state; low output impedance
- Extremely high input resistance; nearly zero steady-state input current
- No direct path steady state between power and ground; no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors