EE141- Spring 2003
Lecture 3
IC Manufacturing

Last Lecture

- Design Metrics (part 1)

Today
- Design metrics (wrap-up)
- IC manufacturing
Administrivia

- Discussion sessions start this week. Only one this week (Dejan is still stuck)
  We 2-3pm in 203 McLaughlin
- Homework 1 due on Th
  » If you have problems running SPICE, check with Huifang
- Labs start next week!
  » Make sure to get your card key coded for 353 Cory
  » Temporary logins have been provided for the PCs in 353 Cory.
    - Login: ee141-temp
    - Password: tempaccount

The EE141 Week at a Glance

<table>
<thead>
<tr>
<th>M</th>
<th>Tu</th>
<th>W</th>
<th>Th</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>Lab (Dejan) 353 Cory</td>
<td>TA mtg BWRC</td>
<td>DISC* Huifang TBD</td>
<td>OH Huifang 289Cory</td>
</tr>
<tr>
<td>Tu</td>
<td>Lec (Jan) 203 McLaughlin</td>
<td>OH (Jan) 511 Cory</td>
<td>DISC* (Dejan) 353 Cory</td>
<td>OH (Dejan) 289Cory</td>
</tr>
<tr>
<td>W</td>
<td>Lab (Huifang) 353 Cory</td>
<td>Lab (Huifang) 353 Cory</td>
<td>OH Huifang TBD</td>
<td></td>
</tr>
<tr>
<td>Th</td>
<td>Lec (Jan) 203 McLaughlin</td>
<td>Lab (both) 353 Cory</td>
<td>Problem Sets Due</td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Discussion sections will cover identical material
Design Metrics (wrap-up)

- How to quantify the quality of a gate?
- So far: cost & reliability
- Today: speed & power

Delay Definitions

- $V_{in}$
- $V_{out}$
- $t_f$
- $t_{PHL}$
- $t_{PLH}$
- 90%
- 50%
- 10%
Ring Oscillator

\[ T = 2 \times t_p \times N \]

A First-Order RC Network

\[ v_{out}(t) = (1 - e^{-t/\tau}) V \]

\[ t_p = \ln (2) \tau = 0.69 \text{ RC} \]

Important model – matches delay of inverter
Power Dissipation

Instantaneous power:
\[ p(t) = v(t)i(t) = V_{\text{supply}}i(t) \]

Peak power:
\[ P_{\text{peak}} = V_{\text{supply}}i_{\text{peak}} \]

Average power:
\[ P_{\text{ave}} = \frac{1}{T} \int_{t}^{t+T} p(t) \, dt = \frac{V_{\text{supply}}}{T} \int_{t}^{t+T} i_{\text{supply}}(t) \, dt \]

Energy and Energy-Delay

Power-Delay Product (PDP) =
\[ E = \text{Energy per operation} = P_{\text{ave}} \times t_{p} \]

Energy-Delay Product (EDP) =
\[ \text{quality metric of gate} = E \times t_{p} \]
A First-Order RC Network

\[
E_{0 \to 1} = \int_0^T P(t) \, dt = V_{dd} \int_0^T i_{\text{supply}}(t) \, dt = V_{dd} \int_0^T V_{\text{dd}} \, dt = C_L \int_0^T V_{\text{out}} \, dt = C_L \cdot V_{\text{out}}^2
\]

\[
E_{\text{cap}} = \int_0^T (p_{\text{cap}}(t) + i_{\text{cap}}(t)) \, dt = V_{\text{dd}} \int_0^T V_{\text{out}} \, dt = \frac{1}{2} C_L \cdot V_{\text{dd}}^2
\]

CMOS Manufacturing Process
CMOS Process

A Modern CMOS Process

Dual-Well Trench-Isolated CMOS Process
Circuit Under Design

This two-inverter circuit (of Figure 3.25 in the text) will be manufactured in a twin-well process.

Circuit Layout
The Manufacturing Process

For a great tour through the process and its different steps, check http://www.fullman.com/semiconductors/semiconductors.html

For a complete walk-through of the process (64 steps), check the Book web-page
http://bwrc.eecs.berkeley.edu/Classes/IcBook

Photo-Lithographic Process

Typical operations in a single photolithographic cycle (from [Fullman]).
Patterning of SiO2

(a) Silicon base material

(b) After oxidation and deposition of negative photoresist

(c) Stepper exposure

(d) After development and etching of resist, chemical or plasma etch of SiO2

(e) After etching

(f) Final result after removal of resist

CMOS Process at a Glance

1. Define active areas
2. Etch and fill trenches
3. Implant well regions
4. Deposit and pattern polysilicon layer
5. Implant source and drain regions and substrate contacts
6. Create contact and via windows
7. Deposit and pattern metal layers
CMOS Process Walk-Through

(a) Base material: p+ substrate with p-epi layer

(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

(c) After plasma etch of insulating trenches using the inverse of the active area mask

(d) After trench filling, CMP planarization, and removal of sacrificial nitride

(e) After n-well and $V_{TP}$ adjust implants

(f) After p-well and $V_{TN}$ adjust implants
CMOS Process Walk-Through

(g) After polysilicon deposition and etch

(h) After $n^+$ source/drain and $p^+$ source/drain implants. These steps also dope the polysilicon.

(i) After deposition of $\text{SiO}_2$ insulator and contact hole etch.

CMOS Process Walk-Through

(j) After deposition and patterning of first Al layer.

(k) After deposition of $\text{SiO}_2$ insulator, etching of via's, deposition and patterning of second layer of Al.
Advanced Metalization

Advanced Metalization
Design Rules

Jan M. Rabaey

3D Perspective

Polysilicon   Aluminum

Gate Oxide   Field Oxide
N+           Source/Drain Regions
P-Type
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - Scalable design rules: lambda parameter
  - Absolute dimensions (micron rules)

CMOS Process Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td></td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td></td>
</tr>
</tbody>
</table>
Layers in 0.25 µm CMOS process

Intra-Layer Design Rules

Same Potential

Different Potential

Well

Active

Select

0 or 6

3

2

10

2

Polysilicon

Metal1

Metal2

Contact or Via Hole

2

3

2

3

3
Transistor Layout

Vias and Contacts
Select Layer

CMOS Inverter Layout
Layout Editor

Design Rule Checker

poly net to all diff minimum spacing = 0.14 um
Sticks Diagram

- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program

Next Lecture

- The inverter at a glance
- The MOS transistor

Stick diagram of inverter