Dynamic operation of MOS transistor
Propagation Delay

Important!

- Homework 2 is due today.
- Homework 3 will be posted today.
Today’s lecture

- The MOS transistor characteristics for transient analysis
- Propagation delay
- Power dissipation

Summary of last lecture

![Graph: Input-output relationship]
Impact of Process Variations

MOS Capacitances
Dynamic Behavior
Dynamic Behavior of MOS Transistor

The Gate Capacitance

\[
C_{\text{Gate}} = \frac{qW}{t_{\text{ox}}} \]

Cross section
Most important regions in digital design: saturation and cut-off
Measuring the Gate Cap

![Gate Capacitance Graph]

Diffusion Capacitance

![Diffusion Capacitance Diagram]

\[ C_{\text{diff}} = C_{\text{bottom}} + C_{\text{bs}} + C_{jx} \times \text{AREA} + C_{jy} \times \text{PERIMETER} \]

\[ = C_{jx} \times W + C_{jy} \times (2L_S + W) \]
Junction Capacitance

Linearizing the Junction Capacitance

Replace non-linear capacitance by large-signal equivalent linear capacitance which displaces equal charge over voltage swing of interest

\[
C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{\text{high}}) - Q_j(V_{\text{low}})}{V_{\text{high}} - V_{\text{low}}} = K_{eq} C_{j0}
\]

\[
K_{eq} = \frac{-\phi_0^m}{(V_{\text{high}} - V_{\text{low}})(1 - m)[(\phi_0 - V_{\text{high}})^{1-m} - (\phi_0 - V_{\text{low}})^{1-m}]}
\]
Capacitances in 0.25 μm CMOS process

<table>
<thead>
<tr>
<th></th>
<th>$C_{ox}$ (F/μm$^2$)</th>
<th>$C_{d}$ (F/μm$^2$)</th>
<th>$C_{j}$ (F/μm$^2$)</th>
<th>$m_j$</th>
<th>$\phi_b$ (F)</th>
<th>$C_{jw}$ (F/μm)</th>
<th>$m_{jw}$</th>
<th>$\phi_{jw}$ (F)</th>
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</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>6</td>
<td>0.31</td>
<td>2</td>
<td>0.5</td>
<td>0.9</td>
<td>0.28</td>
<td>0.44</td>
<td>0.9</td>
</tr>
<tr>
<td>PMOS</td>
<td>6</td>
<td>0.27</td>
<td>1.9</td>
<td>0.48</td>
<td>0.9</td>
<td>0.22</td>
<td>0.32</td>
<td>0.9</td>
</tr>
</tbody>
</table>

**.MODEL Parameters MOS1**

- **.MODEL Modname NMOS/PMOS <VTO=VTO...>**

<table>
<thead>
<tr>
<th>Name</th>
<th>Parameter</th>
<th>Units</th>
<th>Default</th>
<th>Example</th>
<th>Scale Factor</th>
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</thead>
<tbody>
<tr>
<td>VTO</td>
<td>Threshold voltage</td>
<td>V</td>
<td>0</td>
<td>1.0</td>
<td>—</td>
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<tr>
<td>KP</td>
<td>Conductance parameter</td>
<td>AW$^{-2}$</td>
<td>2.0 x 10$^{-9}$</td>
<td>1.0E-3</td>
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<tr>
<td>KOH</td>
<td>Dohrn threshold parameter</td>
<td>V$^{-1}$</td>
<td>0.5</td>
<td>—</td>
<td>—</td>
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<tr>
<td>PHIE</td>
<td>Surface potential</td>
<td>V$^{-1}$</td>
<td>0.6</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>EPHIE</td>
<td>Channel length modulation</td>
<td>V$^{-1}$</td>
<td>1.0E-4</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>RS</td>
<td>Channel sheet resistance</td>
<td>Ω</td>
<td>10</td>
<td>10</td>
<td>—</td>
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<tr>
<td>BS</td>
<td>Source sheet resistance</td>
<td>Ω</td>
<td>10</td>
<td>10</td>
<td>—</td>
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<tr>
<td>BM1</td>
<td>1 and 5 diffusion sheet resistance</td>
<td>Ω</td>
<td>10</td>
<td>10</td>
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<tr>
<td>CBR1</td>
<td>Zero bias BD junction capacitance</td>
<td>F</td>
<td>0</td>
<td>0.3</td>
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<tr>
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<td>0</td>
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<tr>
<td>CT</td>
<td>Zero bias BS junction barrier</td>
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<td>BMJ</td>
<td>Bulk junction grading coefficient</td>
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<td>A</td>
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<tr>
<td>CSUB</td>
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<td>0.1</td>
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<tr>
<td>BMDW</td>
<td>Bulk grading coefficient</td>
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<td>0.33</td>
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<td>BD</td>
<td>Bulk junction potential</td>
<td>V</td>
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<tr>
<td>BS</td>
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<tr>
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<td>CH overlap capacitance per unit</td>
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<td>4.0E-11</td>
<td>W</td>
<td>—</td>
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<tr>
<td>CGSO1</td>
<td>CH overlap capacitance per unit</td>
<td></td>
<td>4.0E-11</td>
<td>W</td>
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<tr>
<td>CGD2</td>
<td>CH overlap capacitance per unit</td>
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<td>2.0E-10</td>
<td>L</td>
<td>—</td>
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<tr>
<td>TLIN</td>
<td>Thin oxide thickness</td>
<td>m</td>
<td>0</td>
<td>0.11</td>
<td>—</td>
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<tr>
<td>ID</td>
<td>Lateral diffusion</td>
<td>m</td>
<td>0</td>
<td>0.20</td>
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</tr>
</tbody>
</table>

EE141
Two Inverters

Two Inverters (modern view)
Computing the Capacitances

The Miller Effect

“A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value.”
Computing the Capacitances

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gd1}$</td>
<td>$2 \cdot CGD0 \cdot W_n$</td>
</tr>
<tr>
<td>$C_{gd2}$</td>
<td>$2 \cdot CGD0 \cdot W_p$</td>
</tr>
<tr>
<td>$C_{dlb1}$</td>
<td>$K_{eh} \cdot (AD_n \cdot CJ + PD_n \cdot CJSW)$</td>
</tr>
<tr>
<td>$C_{dlb2}$</td>
<td>$K_{eh} \cdot (AD_p \cdot CJ + PD_p \cdot CJSW)$</td>
</tr>
<tr>
<td>$C_{g3}$</td>
<td>$c_{ox} \cdot W_n \cdot L_n$</td>
</tr>
<tr>
<td>$C_{g4}$</td>
<td>$c_{ox} \cdot W_p \cdot L_p$</td>
</tr>
<tr>
<td>$C_w$</td>
<td>From Extraction</td>
</tr>
<tr>
<td>$C_L$</td>
<td>$\Sigma$</td>
</tr>
</tbody>
</table>

Propagation Delay
CMOS Inverter Propagation Delay
Approach 1

\[ t_{pHL} = \frac{C_L V_{swing/2}}{I_{av}} \]

\[ \sim \frac{C_L}{k_n V_{DD}} \]

CMOS Inverter Propagation Delay
Approach 2

\[ t_{pHL} = f(R_{on} \cdot C_L) \]

\[ = 0.69 R_{on} C_L \]
Transient Response

\[ t_p = 0.69 \frac{C_L}{(R_{eqn} + R_{eqp})/2} \]

Design for Performance

- Keep capacitances small
- Increase transistor sizes
  » watch out for self-loading!
- Increase \( V_{DD} \) (?)
Delay as a function of $V_{DD}$

\[ t_{\text{III}} = \frac{0.693 C_f V_{DD}^2}{4 I_{DQAIr}} = 0.5 \frac{C_f V_{DD}}{W/L_s k_t k_{in} V_{DQAIr}^2 (V_{DD} - V_{th} - V_{DQA/t/2})} \]

Device Sizing

Self-loading effect: Intrinsic capacitances dominate
NMOS/PMOS ratio

\[ \beta = \frac{W_p}{W_n} \]

Impact of Rise Time on Delay

\[ t_p = t_{\text{step}(i)} + \eta t_{\text{step}(i-1)} \]
The Sub-Micron MOS Transistor

- Threshold Variations
- Subthreshold Conduction
- Parasitic Resistances

Threshold Variations

- Long-channel threshold
  \[ V_T \] as a function of the length (for low \( V_{DS} \))

- Drain-induced barrier lowering
  \[ V_T \] as a function of drain-to-source voltage (for low \( L \))
Sub-Threshold Conduction

The Slope Factor

\[ I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}} \]

\( S \) is \( \Delta V_{GS} \) for \( I_{D2}/I_{D1} = 10 \)

\[ S = n\left(\frac{kT}{q}\right) \ln(10) \]

Typical values for \( S \):

60 .. 100 mV/decade

Sub-Threshold \( I_D \) vs \( V_{GS} \)

\[ I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left( 1 - e^{-\frac{qV_{GS}}{nkT}} \right) \]
Sub-Threshold $I_D$ vs $V_{DS}$

\[ I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left( 1 - e^{\frac{-qV_{GS}}{nkT}} \right) \left( 1 + \lambda V_{DS} \right) \]

$V_{GS}$ from 0 to 0.3V

Next Lecture

- Optimizing for Performance
- Power dissipation in CMOS inverters