1. Objective

There are two primary objectives in this lab. The first objective is to become familiarized with SUE, which is the schematic editor being used in this course. The second is to being laying out some basic building blocks.

Before the lab begins however, it is important that the following question be addressed:

*What is SUE all about and what is all the hype and hoopla over learning it about?*

Before answering this question, one must first understand that a schematic is a symbolic representation of your circuit. It creates a level of abstraction by grouping basic circuit elements (i.e. transistors, capacitors, etc.) into symbols. By doing this, the schematic simplifies the circuit representation into a network of easily recognizable elements by abstracting away from the layout implementation.

As the course progresses, larger and more complex designs than your simple inverter or 2-input NAND gate will be necessary. When the time comes for layout, and several hundred transistors in a jumble of polygons and colors from which no sense can be made (maybe some), it is nice to turn back and utilize the schematic as a guide towards design and verification.

Focusing back on SUE, it is a tool that allows you to create schematics. It has some important and useful features that could prove beneficial later on in the course during debugging such as cross-probing and layout-vs-schematic checking (LVS). Cross-probing in SUE allows you to select a net (a wire with some label/name) in your schematic and see the corresponding net in your MAX layout. Another feature in MAX is hierarchy and abstraction. An example of this would be if you wanted to represent an array of 10 full adder blocks. Instead of having a large layout of polygons, you could create a symbol for a single adder and tile 10 of those together. LVS is a function using algorithms to traverse your layout and schematic and ensure a one-to-one correspondence. Should LVS find mismatches, it will provide output files leading you to your problem. It is also possible to use the schematics from SUE to document certain characteristics of your circuit such as critical path. This can be very useful come crunch time.

The objective of this lab is to first run through the end of the MAX tutorial that makes references to SUE. This should teach you how to input schematics and perform cross-probing. After finishing the tutorial, copy over 3 inverter layouts (links given below). These should be able to fit within the given prboundary (the blue net) without and DRCs. You should also design your gates so that the connections for \( V_{dd} \) and \( G_{ND} \), as well as \( V_{in} \) and \( V_{out} \), all come through the indicated slots in the provided templates.

2. Tasks

a. Read the section about Layout Design Rules, which can be found at the following link:
Keep in mind that all layers have a minimum length, and some layers have enclosure and distance minimums. Take advantage of the real-time DRC checking by looking for the small white dots that represent DRC errors.

b. Layout the CMOS inverter using MAX. The circuit diagram of the inverter is shown in the schematic figure below. Utilize the W/L indicated in the diagram. Please state in your report whether or not you think these sizes are reasonable.

![Schematic diagram of CMOS inverter](http://bwrc.eecs.berkeley.edu/Classes/ICDesign/EE141_f00/Notes/chapter2.pdf)

The file Inverter.max contains the template for this layout. Copy this file, and all other relevant files into your account by executing the following at your UNIX prompt:

```bash
> cp ~ee141/LAB3/*.max .
```

Edit and complete the inverter using MAX. Label the input VIN (using type “input”) and the output VOUT (using type “output”). Also add VDD and GND using a “global” net.

minInverter1.max and minInverter2.max contain the layout area that your inverter should fit into. Add material only within the prboundary. Be sure to add the nwell (the pwell being implicit in this process), and both nwell (nwc) and pwell (pwc) contacts. Complete both layouts and print out your results.

*Note: The contacts are allowed outside the boundary, but all others are not.

d. Go through the rest of the MAX tutorial and become familiarized with SUE’s interface as well as cross-probing. Understanding how Latch.max works is irrelevant at this point, concentrate instead on SUE’s interface and commands.
e. Generate an inverter schematic using SUE. 
Create this schematic using NMOS and PMOS transistors, as well as V_{dd}, GND, and the 
Input and Output nets, which you will label VIN and VOUT respectively.

f. Use the cross-probing features shown in the MAX tutorial to verify that VIN and VOUT 
in your layout correspond with those in your schematic.

3. Report

For your report, please hand in the following:

- Transistor schematics printer from SUE of all your designs
- Printouts of your layouts from MAX of all your designs – Please label all nodes, 
  annotate transistor sizes, and display the grid
- Provide hand calculations of t_{pLH}, t_{pHL}, and t_p
  Use the following parameters:  
  \( V_{in} = 0.43V; V_{ip} = -0.43V; \)  
  \( V_{DSATn} = 0.63V; V_{DSATp} = -1.0V; \)  
  \( k_p = 115 \text{ uA/V}^2; k_n = -30\text{uA/V}^2 \)