The Lumped Model

The Distributed RC-line

Step-response of RC wire as a function of time and space

RC-Models
The Elmore Delay
RC Chain

\[ V_{in} = \frac{N \sum_{i=1}^{N} R_j C_j}{t_{pRC}} \sum_{i=1}^{N} C_i \sum_{j=1}^{N} \]

Driving an RC-line

\[ \tau_D = R_C \tau_{RC} + \frac{R_C}{2} = R_C + 0.5 \tau_{RC} L \]
\[ t_p = 0.69 R_C + 0.38 \tau_{RC} \]

Design Rules of Thumb

- \( \tau_{pRC} \gg \tau_{gate} \) of the driving gate
- \( L_{crit} \gg \sqrt{\tau_{gate}/0.38 \tau_{RC}} \)
- \( \tau_{RC} \gg \) when not met, the change in the signal is slower than the propagation delay of the wire

Inductive Effects in Integrated Circuits

Coaxial Cable
Triplate
Strip Line
MicroStrip
Wire above Ground Plane

L \( \frac{di}{dt} \)
**L di/dt: Simulation**

- **Signals W/charge for Output Driver connected To Bonding Pads**
  - inductance = \( L \)
  - current = \( i_L \)
  - voltage = \( v_L \)

- **Equations**
  - \( v_{out}(t) = \frac{1}{C} \int i_L(t) dt \)
  - \( i_L(t) = \frac{d}{dt} v_{out}(t) \)

**Power Distribution**

- **Supply current is brought on chip at specific locations**
  - on the edge for most chips which are peripherally bonded
  - distributed over the area of the chip for area bonded (C4, solder ball) chips

- **Loads consume this current at different locations on the chip at different times**

- **There is often a large parasitic inductance associated with each bond-wire or solder-ball (0.1-10nH)**

- **Decoupling Capacitors**
  - **EV4 (DEC Alpha 21064, 200MHz)**
    - total effective switching capacitance = 12.5nF
    - 128nF of de-coupling capacitance
    - de-coupling switching capacitance ~ 10x

- **EV5 (DEC Alpha 21164, 300MHz)**
  - 13.9nF of switching capacitance
  - 160nF of de-coupling capacitance

- **EV6 (DEC Alpha 21264, 600MHz)**
  - 34nF of effective switching capacitance
  - 320nF of de-coupling capacitance -- not enough!
EV6 De-coupling Capacitance

Design for $\Delta I_{dd} = 25 A @ V_{dd} = 2.2 V, f = 600 MHz$
- 0.32-$\mu F$ of on-chip de-coupling capacitance was added
  - Under major busses and around major gridded clock drivers
  - Occupies 15-20% of die area
- 1-$\mu F$ 2-$cm^2$ Wirebond Attached Chip Capacitor (WACC) significantly increases "Near-Chip" de-coupling
  - 160 Vdd/Vss bondwire pairs on the WACC minimize inductance

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Lossless Transmission Line - Parameters

Propagation Speed: Only a function of surrounding medium

$\nu = \frac{1}{\sqrt{\varepsilon}} = \frac{1}{\sqrt{\varepsilon_{r} \mu_{0} \mu_{r}^{2}}}$

$\varepsilon_{r}$ permittivity of medium

$\mu_{0}$ permeability of vacuum

Characteristic Impedance $= \frac{1}{\nu \varepsilon_{0} \omega}$

$100$ to $500$ $\Omega$ for typical wires

Ev6 WACC

389 Signal - 198 VDD/VSS Pins
- 389 Signal Bondwires
- 395 VDD/VSS Bondwires
- 320 VDD/VSS Bondwires

Wave Propagation Speed

<table>
<thead>
<tr>
<th>Diodielectric</th>
<th>$\varepsilon_{r}$</th>
<th>Propagation Speed (nsecs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vacuum</td>
<td>1</td>
<td>50</td>
</tr>
<tr>
<td>Micron</td>
<td>1.9</td>
<td>15</td>
</tr>
<tr>
<td>FR Board (Spay Glass)</td>
<td>5.8</td>
<td>13</td>
</tr>
<tr>
<td>Absorber (Ceramic Package)</td>
<td>9.5</td>
<td>10</td>
</tr>
</tbody>
</table>

Didodielectric Constants and Wave Propagation Speeds for Various Materials, Used in Electronic Circuits (from [Bakhsh09]).

Wave Reflection for Different Terminations

Wave Equation

$\frac{1}{\varepsilon} - i \frac{\varepsilon}{\omega} - i \frac{\varepsilon}{\omega} - \frac{i}{\varepsilon_{0} \omega}$

Reflection Coefficient

$R = \frac{V_{inc} + V_{refl}}{V_{inc} - V_{refl}}$

$V_{inc}$ incident voltage

$V_{refl}$ reflected voltage

$R_{inc}$ input reflection coefficient

$R_{refl}$ output reflection coefficient
Transmission Line Response ($R_L = \infty$)

Lattice Diagram

Design Rules of Thumb

- Transmission line effects should be considered when the rise or fall time of the input signal ($t_r, t_f$) is smaller than the time-of-flight of the transmission line ($t_{\text{flight}}$).
  
  \[ t_r, t_f \ll 2.5 t_{\text{flight}} \]

- Transmission line effects should only be considered when the total resistance of the wire is limited:
  
  \[ R < 5 Z_0 \]

- The transmission line is considered lossless when the total resistance is substantially smaller than the characteristic impedance,
  
  \[ R < Z_0/2 \]