Sequential Logic

2 storage mechanisms
- positive feedback
- charge-based
Latch versus Flip-Flop

- **Latch**
  - stores data when clock is low

- **Flip-Flop**
  - stores data when clock rises

Positive Feedback: Bi-Stability
Meta-Stability

Gain should be larger than 1 in the transition region

Mux-Based Latches

Negative latch (transparent when CLK= 0)  Positive latch (transparent when CLK= 1)
Mux-Based Latch

(a) Schematic diagram

(b) Non-overlapping clocks

Pseudo-static Latch

SR Latch

CMOS Clocked SR Latch

Latch: Transistor Sizing
6 Transistor CMOS SR Latch

Race Problem

Signal can race around during $\phi = 1$. 
Latch-Based Design

- N latch is transparent when $\phi = 0$
- P latch is transparent when $\phi = 1$

Master-Slave Latch Pair

Mux based
Master-Slave Flip-Flop

2-phase dynamic flip-flop
Master-Slave Flip-Flop

Overlapping Clocks Can Cause
- Race Conditions
- Undefined Signals

2 phase non-overlapping clocks
2 phase non-overlapping clocks

Flip-flop insensitive to clock overlap
Flip-Flop: Timing Definitions

Delay vs. Setup/Hold Times
Pulse-Triggered Latches

Flip-flops:

Master-Slave Latches

Pulse-Triggered Latch

Propagation Delay Based Edge-Triggered

Mono-Stable Multi-Vibrator
**Pulse-Triggered Latches**

Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7:

![Hybrid Latch - Flip-flop (HLFF)](image)

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**7474, SR latch as a second stage**

![7474, SR latch as a second stage](image)
Pulse-Triggered Latches

Sense-amplifier-based flip-flop, DEC Alpha 21264, StrongARM 110

- First stage is a sense amplifier, precharged to high, when $Clk = 0$
- After rising edge of the clock, sense amplifier generates the pulse on $S$ or $R$
- The pulse is captured in S-R latch
- Cross-coupled NAND has different propagation delays of rising and falling edges

Maximum Clock Frequency

Also:

$t_{del} + t_{delay} > t_{hold}$

$t_{del}$: contamination delay = minimum delay
Pipelining

Non-pipelined version

Pipelined version

<table>
<thead>
<tr>
<th>Clock Period</th>
<th>Adder Value</th>
<th>Absolute Value</th>
<th>Logarithm</th>
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<tr>
<td>1</td>
<td>$a_1 + b_1$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>$a_2 + b_2$</td>
<td>$</td>
<td>a_1 + b_1</td>
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<tr>
<td>3</td>
<td>$a_3 + b_3$</td>
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<td>4</td>
<td>$a_4 + b_4$</td>
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<tr>
<td>5</td>
<td>$a_5 + b_5$</td>
<td>$</td>
<td>a_4 + b_4</td>
</tr>
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</table>

Pipelined Logic using C²MOS

What are the constraints on $F$ and $G$?
Example

Number of a static inversions should be even

NORA CMOS Modules

(a) φ-module

(b) φ-module
**TSPC - True Single Phase Clock Logic**

- Precharged N
- Precharged P
- Non-precharged N
- Non-precharged P

Incorporating logic into the latch and inserting logic between latches.

Digital Integrated Circuits
Sequential Logic
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Doubled TSPC Latches

Doubled n-TSPC latch

Doubled p-TSPC latch

TSPC - True Single Phase Clock Logic

Including logic into the latch

Inserting logic between latches
Master-Slave TSPC Flip-flops

(a) Positive edge-triggered D flip-flop
(b) Negative edge-triggered D flip-flop
(c) Positive edge-triggered D flip-flop using split-output latches

Schmitt Trigger

- VTC with hysteresis
- Restores signal slopes
Noise Suppression using Schmitt Trigger

CMOS Schmitt Trigger

Moves switching threshold of first inverter
Schmitt Trigger
Simulated VTC

CMOS Schmitt Trigger (2)
Multivibrator Circuits

- **Bistable Multivibrator**: flip-flop, Schmitt Trigger
- **Monostable Multivibrator**: one-shot
- **Astable Multivibrator**: oscillator

Transition-Triggered Monostable

In

DELAY

Out

t_d

In

Out

t_d
Monostable Trigger (RC-based)

(a) Trigger circuit.

(b) Waveforms.

Astable Multivibrators (Oscillators)

Ring Oscillator

simulated response of 5-stage oscillator
Voltage Controller Oscillator (VCO)

Relaxation Oscillator

\[ T = 2 \log_3 RC \]