EECS 141 – F01
Lecture 6

Power Dissipation
Where Does Power Go in CMOS?

- **Dynamic Power Consumption**
  Charging and Discharging Capacitors

- **Short Circuit Currents**
  Short Circuit Path between Supply Rails during Switching

- **Leakage**
  Leaking diodes and transistors

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Dynamic Power Dissipation

Energy/transition = $C_L \times V_{dd}^2$

Power = Energy/transition $\times f = C_L \times V_{dd}^2 \times f$

- Not a function of transistor sizes!
- Need to reduce $C_L$, $V_{dd}$, and $f$ to reduce power.
Modification for Circuits with Reduced Swing

\[ E_0 \rightarrow 1 = C_L \cdot V_{dd} \cdot (V_{dd} - V_t) \]

- Can exploit reduced swing to lower power (e.g., reduced bit-line swing in memory)

Adiabatic Charging

\[ C \frac{d^2 v_c}{dt^2} = \frac{V_{dd}}{2} \]

Consider

\[ v_c = \frac{1}{C} \int_0^t i(t) dt + \frac{1}{C} i_{in} \cdot \tau \]

\[ \tau_{sv} = \frac{C \cdot v_c}{V_{dd}} \]

\[ E_{diss} = R \int_0^t i(t)^2 dt \leq R \int_0^t i_{sw}^2 dt = R \cdot \frac{1}{2} i_{sw}^2 \cdot \tau = \frac{R \cdot C \cdot v_c^2}{2} \]

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Adiabatic Charging

\[ V_L = RI_v + V_C = \frac{dv}{dt} + V_C \]

\[ V_I = \text{cst} \rightarrow \text{Exponential current} \quad I = I_{\text{lin}} \rightarrow \text{Linear ramp on } V_I \]

\[ E_R = CV_c^2/2 \]

Node Transition Activity and Power

- Consider switching a CMOS gate for \( N \) clock cycles

\[ E_N = C_L \cdot V_{dd}^2 \cdot n(N) \]

\( E_N \) : the energy consumed for \( N \) clock cycles

\( n(N) \) : the number of 0->1 transition in \( N \) clock cycles

\[ P_{avg} = \lim_{N \to \infty} \frac{E_N}{N} \cdot f_{\text{clk}} = \left( \lim_{N \to \infty} \frac{n(N)}{N} \right) \cdot C_L \cdot V_{dd}^2 \cdot f_{\text{clk}} \]

\[ \alpha_{0 \to 1} = \lim_{N \to \infty} \frac{n(N)}{N} \]

\[ P_{avg} = \alpha_{0 \to 1} \cdot C_L \cdot V_{dd}^2 \cdot f_{\text{clk}} \]
Short Circuit Currents

How to keep Short-Circuit Currents Down?

Short circuit current goes to zero if $t_{\text{fall}} \gg t_{\text{rise}}$, but can’t do this for cascade logic, so ...
Minimizing Short-Circuit Power

- Keep the input and output rise/fall times the same (< 10% of Total Consumption) from [Veendrick84] (IEEE Journal of Solid-State Circuits, August 1984)
- If $V_{dd} < V_{tn} + |V_{tp}|$ then short-circuit power can be eliminated!

Leakage

Sub-threshold current one of most compelling issues in low-energy circuit design!
Reverse-Biased Diode Leakage

\[ I_{DL} = J_S \times A \]

- \( J_S = 1-5 \text{pA/}\mu\text{m}^2 \) for a 1.2\mu m CMOS technology
- \( J_S \) doubles with every 9°C increase in temperature

Subthreshold Leakage Component

- Leakage control is critical for low-voltage operation
**Static Power Consumption**

\[ P_{\text{stat}} = P_{(I_{\text{n}}=1)} \cdot V_{\text{dd}} \cdot I_{\text{stat}} \]

Should be avoided in most cases, but could help reducing energy in others (e.g. sense amps)

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**Principles for Power Reduction**

- **Prime choice: Reduce voltage!**
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages (0.6 … 0.9 V by 2010!)
  - Maintaining performance by threshold scaling leads to increased leakage
- **Reduce switching activity**
- **Reduce physical capacitance**