1. Objective

The main objective of this lab is to familiarize you with the procedure to extract a SPICE netlist from MAX and to prepare and analyze the simulation.

2. Tasks

**Part 0:**

a. Create a lab4 directory, and copy over Inverter.max and Inverter.sue from your lab3 directory. Also copy MyNAND.sue to your lab4 directory. MyNAND.sue is located in $MMI_TOOLS/tutorials/max/MyNAND.sue

**Part 1:**

a. Open the inverter layout in MAX and extract the layout by clicking local/"extract it" on the menu. If you look in your directory again, you notice that there is now a file called Inverter.ext, which is the extraction of your circuit.

b. Using this extraction, it is now possible to obtain a SPICE netlist by using the command ext2spice. This will convert the extraction to a usable netlist. To do this, type in the following at your command prompt. Be sure you are in your lab4 directory.

```
> cp ~/ee141/LAB4/ext2spice .
> ./ext2spice --n Inverter
```

(Note: there is no .ext extension)

Open up the resulting Inverter.spice file. Note that the widths and lengths are well off what they actually should be and that the source and drain areas, as well as perimeter are incorrect. You need to hand modify these parameters using your favorite text editor. Selecting the rectangular region and noting the dimensions in the bottom right hand corner of MAX allows you to calculate the area and perimeter. Save your modified netlist as Inverter.sp

c. Simulate the extracted SPICE netlist to obtain the transient response and the DC transfer characteristics. Use Vdd = 2.5V. The netlist you obtain from extraction will only give you the two transistors. You will have to add the rest of the code for a simulation to run. Using your results, obtain the following: $V_{OH}$, $V_{OL}$, $V_{HI}$, $V_{IL}$, $V_{M}$, $NM_H$, $NM_L$ from the VTC, and $t_{plh}$ and $t_{phl}$ from the transient analysis.

*Turn in:* Layout, extracted SPICE deck, edited SPICE deck, VTC and transient plots, and your calculated values.
d. Add a 50fF load capacitor in your SPICE deck. Now resize your transistors so that the new circuit will have a transient response within 10% of the original. Modify your layout to reflect these changes, re-extract, and re-simulate. The book’s draft chapters offer methods by which the new dimensions can be determined.

*Turn in: Your new layout, SPICE deck, transient plots, and your calculated $\tau_{plh}$ and $\tau_{phl}$. Please qualitatively explain your reasoning for the transistor sizing, and hand in your hand analysis.

Part II:

The following steps are in preparation to use the IRSIM switch level simulator, which will allow you to get an idea of the functional operation of a circuit. IRSIM is currently not working, but we want you to prepare what you would have had to.

a. Copy over .suerc from the ~ee141/LAB4 directory using the following command in your lab4 directory:

```bash
> cp ~ee141/LAB4/.suerc .
```

b. Open the Inverter.sue in your lab4 directory. Click on Sim/"Change Simulation Mode” on the menu and change the mode to type sim. Now create a sim Netlist by either clicking Sim/"sim netlist” or pressing “Shift-N”. This will create Inverter.sim in your directory. Print this out and include it in your report.

*Note: Double click on the transistors in the schematic and make sure that the NMOS and PMOS dimensions are in terms of $ln_{min}$ and $lp_{min}$. Make sure that the widths are multiples of these (i.e. width expressed as “2” as opposed to “0.48 u”)

c. Now open MyNAND.sue in your lab4 directory. Repeat step b for this schematic.

Qualitatively explain how the NAND gate operates under all possible input conditions. The $\tau_{plh}$ will be different depending on input conditions. Under what condition will the output rise fastest? Why? Please answer this in your report.

3. Report

For your report, please hand in the following:

- Printouts of your schematics from SUE and layouts from MAX
- Printouts of your SPICE input decks (extracted and edited)
- The manual calculations for the parameters determined in Part I.
- A comparison between your hand analysis and SPICE, along with an explanation of the differences.
- Qualitative reasoning and hand calculations used in your decision for the transistor sizing in Part I
- Inverter.sim and MyNAND.sim printouts
- Explanation of NAND gate operation and answer to the $\tau_{phl}$ question

Enjoy your light week of lab! Good luck on your 141 midterm next week (October 4)!