Problem #1 Propagation Delay and Energy

a) What is the delay of a minimum sized inverter driving another inverter $f$ times its size? For the minimum sized inverter, assume input capacitance equal to $C_{\text{unit}}$, equivalent resistance through the NMOS or PMOS equal to $R_{\text{unit}}$, and intrinsic (self-loading) capacitance on the output also equal to $C_{\text{unit}}$. Assume that the capacitance and resistance values scale linearly with size. Your answer will be in terms of these parameters (no calculations!). Take the limit as $f$ goes to 0 and call the result $\tau_{\text{inv}}$.

$$\tau_p = 0.69R_{\text{unit}}C_{\text{unit}} (1+f)$$
As $f$ goes to zero,
$$\tau_{\text{inv}} = 0.69R_{\text{unit}}C_{\text{unit}}$$

b) From part a), how much energy is consumed by the driving inverter after successive low to high ($L\rightarrow H$) and high to low ($H\rightarrow L$) transitions, in terms of a supply voltage $V_{\text{dd}}$?

Energy $= C_{\text{unit}} (1+f) V_{\text{dd}}^2$

c) In order to drive a large capacitance ($CL=60C_{\text{unit}}$) from a minimum size gate (with input capacitance $C_{\text{in}}= C_{\text{unit}}$), you decided to introduce a two-stage buffer as shown in Fig. 1. From (a), the propagation delay of a self-loaded minimum size inverter is $\tau_{\text{inv}}$. Assume that the capacitance and resistance values scale linearly with size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay. What is the corresponding propagation delay?

We want to size the buffers geometrically.

$$f = (60/1)^{1/3} = 3.915$$

$$\tau_p = N\tau_{\text{inv}} (1+f) = 14.745 \tau_{\text{inv}}$$

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**Fig. 1: Buffer Chain**
d) Given a supply voltage of Vdd, what is the energy-delay product of the circuit in part (c)?

\[ PDP = \frac{1}{2} C Vdd^2 = \frac{1}{2} \left( 2 \left( C_{\text{unit}}(1 + f + f^2) \right) + C_L \right) Vdd^2 \]
\[ EDP = \frac{1}{2} E^* \tau_p = 591.58 \ C_{\text{unit}} \ \tau_{\text{inv}} \ Vdd^2 \]

\[ \tau_p = \tau_{\text{inv}} \left[ (1+f) + (1+f) + (1+60/f^2) \right] = (3 + 2f + 60/f^2) \]
\[ 14.745 \ \tau_{\text{inv}} < \tau_p < 1.1 * 14.745 \ \tau_{\text{inv}} \]
\[ 11.745 < 2f + 60/f^2 < 13.2195 \]
Take the upper bound
\[ f = 2.8098 \]
\[ EDP = \frac{1}{2} E^* \tau_p = 676.43 \ C_{\text{unit}} \ \tau_{\text{inv}} \ Vdd^2 \]

f) Find the optimum number of inverters and sizing ratio for the output load specified in Part (c). Express the optimum delay in terms of \( \tau_{\text{inv}} \). Considering your result for Part (b), do you think this inverter chain will consume more or less energy than a single inverter driving the output load?

For this problem, it’s easiest just to plug in numbers for a few values (with \( f = 60^{1/N} \) and delay proportional to \( N(1+f) \) as in part (c)). The optimal number of inverters is then 3, with sizing ratio 3.915, corresponding to a delay 14.74\( \tau_{\text{inv}} \).

<table>
<thead>
<tr>
<th>N</th>
<th>f</th>
<th>N(1+f)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>60</td>
<td>61</td>
</tr>
<tr>
<td>2</td>
<td>7.746</td>
<td>17.492</td>
</tr>
<tr>
<td>3</td>
<td>3.915</td>
<td>14.74</td>
</tr>
<tr>
<td>4</td>
<td>2.783</td>
<td>15.133</td>
</tr>
</tbody>
</table>

If you play around with the size of the load, you will see that the N which corresponds to f closest to 4 results in the smallest delay. That is why we say that a fanout of 4 (FO4) is typically best.

You can also directly find N that give f=4:

\[ 4 = (F)^{1/N} \Rightarrow N = \frac{\ln(F)}{\ln(4)} = 2.95 \]
At this point, the easiest way to determine whether to use \( N=2 \) or \( N=3 \) is to compute the delay in both cases and compare the results.

Regardless of the number of inverters in the chain, the final load capacitance \( C_L \) has to be switched, contributing \( C_L V_{dd}^2 \) to the total energy. To minimize the total energy, we then would want to minimize the transistor contribution to the capacitance, which would mean using a single minimum sized inverter. As with many minimum energy solutions, this comes at a significant delay penalty.

**Problem #2: Power Dissipation**

Consider the “source follower” circuit used to drive a load \( C_L=50fF \) shown above. M1 and M2 are both NMOS transistors parameterized by Table 3-2 on page 103 in the text, and \( 2\Phi_f = -0.6V \).

The inverter is a standard CMOS inverter. Assume that the input square wave edges and the inverter are fast compared to the rest of the circuit.

(a) Assuming that \( T \) is relatively long compared to \( t_{PLH} \) and \( t_{PHL} \), sketch the transient waveforms of \( V_{IN} \) and \( V_{OUT} \) over a couple of cycles.

The overall function of this circuit is a follower. When \( V_{IN} \) is low, M1 is off and M2 is on, and the \( V_{OL} = 0 \) V. When \( V_{IN} \) is high, M2 is off and M1 is on and in a “source follower” configuration. As \( V_{OUT} \) rises, it eventually reaches \( V_{DD} - V_T \), at which point M1 turns off. Therefore, \( V_{OH} = V_{DD} - V_T \). However, since \( V_{SB} \) is not equal to 0, \( V_T \) is not equal to \( V_{TO} \). We need to find \( V_T \) from the two equations:

\[
V_T = \beta_T \left( \sqrt{-2\Phi_f + V_{AS}} - \sqrt{-2\Phi_f} \right), \quad V_{AS} = V_{DD} - V_T
\]
A simple way to solve these equations is to iterate with an initial guess for $V_T$, for example, 0.5 V.

- $V_{SB} = 2.0 \text{ V}$
- $V_T = 0.835 \text{ V} \quad V_{SB} = 1.665 \text{ V}$
- $V_T = 0.720 \text{ V} \quad V_{SB} = 1.78 \text{ V}$
- $V_T = 0.737 \text{ V} \quad V_{SB} = 1.763 \text{ V}$

At this point we are close to the final value, and the last few mV don’t affect the solution significantly. Use $V_{OH}=1.76 \text{ V}$. Now we can sketch the input and output waveforms:

![Waveform Diagram]

b) What is the power consumption if $T=50\text{ ns}$? Neglect the standard inverter and assume that $C_L$ dominates the device capacitance of M1 and M2.

Note that during a $0 \rightarrow 1$ transition, we charge the capacitor to $V_{OH}$, and thus draw an amount of charge $Q = C_L V_{OH}$ from the supply. Thus, the energy consumed in a single positive transition is $E = QV_{DD} = C_L V_{DD} V_{OH}$. Therefore,

$$P = C_L V_{DD} V_{OH} f_{0 \rightarrow 1} = 50 \text{ fF} \times 2.5 \text{ V} \times 1.76 \text{ V} \times 10 \text{ MHz}.$$  

$P = 2.2 \mu\text{W}$

c) Consider what happens if $V_{IN}$ is not a square wave, but a data stream consisting of a random sequence of bits. If the bit period is 50 ns and each bit has an equal chance of being 0 or 1, what is the average power consumption of the circuit?

In this case we use the same power formula as in part (b), but we must determine the new value of $f_{0 \rightarrow 1}$. Since the bits have equal probability of being 0 or 1, every bit has a 50% chance of being different from the previous bit. Thus, on average there is a transition every 100 ns. Half of those transitions are $0 \rightarrow 1$ and half are $1 \rightarrow 0$, so on average there is a $0 \rightarrow 1$ transition every 200 ns, or $f_{0 \rightarrow 1} = 5 \text{ MHz}$.

$$P = C_L V_{DD} V_{OH} f_{0 \rightarrow 1} = 50 \text{ fF} \times 2.5 \text{ V} \times 1.76 \text{ V} \times 5 \text{ MHz}.$$  

$P = 1.1 \mu\text{W}$