Problem #1

A two stage buffer is used to drive a metal wire of 1 cm. The first inverter is a minimum size with an input capacitance $C_i = 10 \text{ fF}$ and a propagation delay $t_{p0} = 175 \text{ ps}$ when loaded with an identical gate. The width of the metal wire is $3.6 \mu\text{m}$. The sheet resistance of the metal is $0.08 \Omega/\square$, the capacitance value is $0.03 \text{ fF}/\mu\text{m}^2$ and the fringing field capacitance is $0.04 \text{ fF}/\mu\text{m}$.

a. What is the propagation delay of the metal wire?

$$R = 0.08 \Omega/\square \times (1\text{cm} / 3.6\mu\text{m}) = 222 \Omega$$

$$C_{pp} = 0.03 \text{ fF}/\mu\text{m}^2 \times (3.6 \mu\text{m}) \times (10000 \mu\text{m}) = 1.08 \text{ pF}$$

$$C_{fringe} = 2 \times 0.04 \text{ fF}/\mu\text{m} \times 10000 \mu\text{m} = 0.80 \text{ pF}$$

$$C_{wire} = C_{pp} + C_{fringe} = 1.88 \text{ pF}$$

**Lumped** RC model

$$t_p = 0.69 \frac{RC_{wire}}{2} = 288 \text{ ps}$$

**Distributed** RC model,

$$t_p = 0.38 \frac{RC_{wire}}{2} = 159 \text{ ps}$$

b. Compute the optimal size of the second inverter as to minimize the total delay. What is this minimum delay through the buffer?

The circuit given in this part of the problem looks like this:

![Two-stage buffer driving a wire.](image)

**Figure 1. Two-stage buffer driving a wire.**

To find the minimum delay, we start from the delay expression:

$$t_p = t_{p0}(1 + x) + t_{p0}(1 + C_{wire}/xC_i) = \text{minimum}$$

$$\frac{\partial t_p}{\partial x} = 0 \Rightarrow x = \sqrt{C_{wire}/C_i} = 13.7$$

The total buffer delay is then given by: $t_{p,buffer} = 2 \cdot (1 + x) \cdot t_{p0} = 5.5 \text{ ns}$

Answer $t_{p,buffer} = 2.75 \text{ ns}$ is also acceptable (if you took $t_{p0}/2$ to be actual $t_{p0}$)
Problem #2

Calculate the Elmore delay from node A to node B using the values for the resistors and capacitors given in the table below.

First, let’s label all the nodes:

Following the formula for Elmore delay in Chapter 4 of the book, (Equations 4.12 and 4.13), we first calculate the $R_{IB}$ for each node (results in table below).

<table>
<thead>
<tr>
<th>common resistance from A to Node and B</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{BB}$</td>
</tr>
<tr>
<td>$R_{CB}$</td>
</tr>
<tr>
<td>$R_{DB}$</td>
</tr>
<tr>
<td>$R_{EB}$</td>
</tr>
<tr>
<td>$R_{FB}$</td>
</tr>
<tr>
<td>$R_{GB}$</td>
</tr>
<tr>
<td>$R_{HB}$</td>
</tr>
<tr>
<td>$R_{IB}$</td>
</tr>
</tbody>
</table>

Using Eq. (4.13) from the textbook, we obtain $\tau = 252.25\text{ps}$. The propagation delay is given by:

$$t_p = 0.69 \tau = 174\text{ ps}$$

Let’s check with SPICE to see how accurate our answer is. We expect the 0%-90% rise time to be $t_{rise} = \tau \ln \left( \frac{V_{swing}}{V_{swing} - 0.9V_{swing}} \right) = \tau \ln(10) = 2.3*\tau = 580\text{ps}$. 


Here’s the spice deck describing our network.

* rc elmore network
  R1 a c 0.25
  R2 c d 0.25
  R3 c e 0.50
  R4 c f 100
  R5 e g 0.25
  R6 e h 1
  R7 e i 0.75
  R8 h b 1000
  C1 c 0 250f
  C2 d 0 750f
  C3 e 0 250f
  C4 f 0 250f
  C5 g 0 1000f
  C6 h 0 250f
  C7 i 0 500f
  C8 b 0 250f

Vin a 0 pulse 0 2.5 2n lp lp 10n 30n

.TRAN 0.5p 40n
.OPTIONS post=2 nomod

.END

Below is the plot of input and output. We see that the 0%-90% rise time is 580ps, which agrees perfectly with our prediction!
Problem #3

a) "Critical length" of the wire

Approximate the driver as a voltage source in series with a resistor $R_S$:

$$ R_S \approx \frac{R_N + R_S}{2} = 5 k\Omega $$

(2.1)

![Diagram of voltage source in series with a resistor](image)

The “critical length” is when the delay from the wire resistance is the same as the delay added by the wire capacitance alone. Using wire model shown below,

![Diagram of wire model](image)

and using the Elmore delay equations, we obtain the Elmore delay (i.e. time constant) at node $x$:

$$ \tau_x = \frac{C_w}{2}(R_S) + \frac{C_w}{2}(R_S + R_w) = R_S C_w + \frac{R_w C_w}{2} $$

(2.2)

As discussed in the class $R_S C_w$ is the delay due to the wire capacitance, and $R_w C_w/2$ is the delay due to the wire resistance. The critical delay is achieved when these two delays are equal, which occurs when $L = 2 R_S / r$.

$$ r = \frac{80 m\Omega / \mu m}{0.5 \mu m} = 0.16 \Omega / \mu m $$

(2.3)

(2.1) & (2.3) $\Rightarrow$ $L = 62.5 \text{ mm}$

More accurately: $L = 0.69 / 0.38 \times R_S / r = 1.8 R_S / r \Rightarrow L = 56.25 \text{ mm}$

b) Equivalent capacitance of a wire of length $L$

Equivalent capacitance is the sum of parallel-plate and fringing capacitance.

- $C_{pp} = 30 \text{ aF/\mu m}^2 \times (0.6 \mu m) \times (62.5 \text{ cm}) = 11.25 \text{ pF}$
- $C_{fringe} = 2 \times (40 \text{ aF/\mu m}) \times 62.5 \text{ cm} = 50 \text{ pF}$ (don’t forget factor 2!)

$C_{wire} = C_{pp} + C_{fringe} = 61.25 \text{ fF}$
Problem #4

a) **Fixed voltage scaling.** Geometry scaling factor: \( S = 0.18\mu m / 0.13\mu m = 1.38 \)

Area: \( A' = A/S^2 = 0.37\text{mm}^2 \)

Power: \( P' = 0.4\text{mW/MHz} \times 100\text{MHz} \times 1/S = 29\text{mW} \)

Note: power would have been 40mW had we not reduced the frequency.

Power density: \( PD = P'/A' = 78.4\text{mW/mm}^2 \)

b) **General scaling.** \( U = 1.8/1.2 = 1.5 \)

Power: \( P = P'/U^2 = 40\text{mW}/2.25 = 17.78\text{mW} \)

Power density: \( PD = P'/A' = 48.05\text{mW/mm}^2 \)

If you assumed a 100MHz operation, Power = 12.9mW, PD = 34.8 mW/mm².

c) **General scaling from (b).**

Maximum operating frequency: \( f' = S \times f = 150\text{MHz} \)

Power and Power Density are the same as in part (b) since the effects of increased frequency (by a factor \( S \)) and decreased capacitance (by a factor \( 1/S \)) cancel out. Therefore,

\[
\text{Power:} \quad P_{150\text{MHz}} = P_{(b)} = 17.78\text{mW} \\
\text{Power Density:} \quad PD_{150\text{MHz}} = PD_{(b)} = 48.05 \text{ mW/mm}^2
\]

d) **Maintaining power density.**

\[
PD = P/A \sim (1/U^2)/(1/S^2) = S^2/U^2
\]

\[\Rightarrow U = S = 1.38\]

\[\Rightarrow V' = 1.8/U = 1.3V\]

Note: General voltage scaling assumed \( U > S \), which resulted in lower power density than in the original design. To keep power density the same, \( U \) has to decrease a bit, resulting in a higher voltage (1.3V vs. 1.2V in general scaling).

Problem #5

Since no assumption has been made about relative width-to-height ratio of the wire, we assume general model which considers both parallel plate and fringing components. Capacitance of such a wire, **per unit length**, is modeled using following expression:

\[
C_{wire} = C_{pp} + C_{fringe} = \varepsilon_{di} W t_{di} + \frac{2\pi \varepsilon_{di}}{\log \left( \frac{t_{di}}{H} \right)}
\]

(5.1)

where \( W \) is the width of the wire, \( t_{di} \) is the thickness of the dielectric, and \( H \) is the height (or thickness) of the wire. From Eq. (5.1), we can derive following results.

I. \( E \) \( (C_{pp} \text{ increases with } W \text{ by unknown factor since } C_{pp}/C_{fringe} = ?) \)

II. \( C \) \( (\text{both } R \text{ and } C \text{ decrease by } 2x, \text{ so } RC \text{ decreases by } 4x) \)

III. \( E \) \( (\text{unknown scaling factor for } C \text{ since } C_{pp}/C_{fringe} = ?) \)

IV. \( E \) \( (\text{same explanation as III}) \)