Problem 1 – Logic with Pass Transmission Gate

Following is the original figure with a few annotations to help explain the operation:

1A \[ F = A \oplus B \]

When signal A is high, A’ is low. The transmission gate formed by transistor pair P2 and N2 is open. Transistor pair P1 and N1 thus acts as an inverter, with B’ appearing at the output.

When signal A is low, A’ is high. The transmission gate (P2, N2) is now closed, passing B to the output. The inverter (P1, N1) is disabled.

1B Dynamic logic is inverting in nature, so you need an inverter at the output to get your output to be logically correct. This is just one way to do it, and there are other possible correct answers.

This version is the pull-down NMOS version of the XOR function. Precharge happens when the clock signal is low, pre-pulling the intermediate signal high. Evaluation occurs when the clock signal is high. The intermediate node x either remains charged at its previous value or gets pulled down to ground.
This version is the pull-up PMOS version of the XOR function. Predischarge happens when the clock signal is high, pre-pulling the intermediate node low. Evaluation occurs when the clock signal is low. The intermediate node \( x \) either remains charged at its previous value or gets pulled up to VDD.

**Problem 2 – Dynamic Logic**

2A

\[
F = AB + AC_in + BC_in
\]
\[
G = A \oplus B \oplus C_in
\]

Both gates are evaluating when CK is low.

During this period inputs are not allowed to change (only low to high transition would be allowed in the calculation of F while only high to low transition would be allowed in the calculation of G; clearly, one of these two conditions would be violated if inputs change during CK = low). Therefore, inputs are allowed to change only when CK = high.

2B It can be easily observed that F is the function of carry out, while G carries the function of output sum. Thus the gate implements full adder function.

2C M1 predischarges the evaluation node \((A' + B' + C_in)\) to ensure there is no charge sharing between this node and G. Otherwise, erroneous high values may occur.

2D Move \( C_in \) transistor closer to the output as shown on the right. This change improves the delay because \( C_in \) is the last signal to settle.
2E No. The transistor placement is already optimized for G computing.

Problem 3 – Charge Sharing Analysis

There’s two possible cases.

1) If $V_{out}$ changes by more than $V_{Tn}$.
2) If $V_{out}$ changes by less than $V_{Tn}$.

The charge is split between “two” capacitors. The one at the load, $C_L = 36\,$fF (30\,fF external + 6\,fF gate parasitic), and the internal capacitance seen at node X. The capacitance at node X as far as this problem is concerned is equivalent to 3 drain-to-bulk capacitances and 1 source-to-bulk capacitance for a total of $12\,$fF.

Case 1: $\Delta V_{out} < V_{Tn}$

$$\Delta V_{out} = -\frac{C_x}{C_L} [V_{DD} - V_{Tn}] = -\frac{12}{36} [2.5 - 0.5] = -0.67\,$V$$

In this case, the final value of $V_{out}$ is 1.83V.

Case 2: $\Delta V_{out} > V_{Tn}$

$$\Delta V_{out} = -\frac{C_x}{C_L + C_x} (V_{DD}) = -\frac{12}{48} (2.5) = -0.625\,$V$$

In this case, the final value of $V_{out}$ is 1.875V.

$$\frac{C_x}{C_L} \geq \frac{V_{Tn}}{V_{DD} - V_{Tn}} \Rightarrow 0.33 \geq 0.25 \quad \text{(see textbook pg. 293)}$$

Thus, case 2 holds.

$V_{out} = 1.875\,$V
Problem 4 – Combinational Logic and Logical Effort

4A

The complementary CMOS implementation is to the left. Logical effort is defined as the ratio of input capacitance of a gate (considering only one input) to the input capacitance of an inverter with the same output current. This gives us:

\[ g_A = \frac{2+2}{2+1} = \frac{4}{3} \]

\[ g_B = \frac{4+2}{2+1} = 2 \]

\[ g_C = \frac{4+2}{2+1} = 2 \]

Figure 1. XNORT path.

4B

The transition probability of the gate is

P(F:0 \rightarrow 1) = P(F=0)P(F=1) = \frac{3}{8} \cdot \frac{5}{8} = \frac{15}{64} \approx 0.23

The transition probability of a two-input NOR (again with all inputs assumed equally likely) is \(3/16 \approx 0.19\), lower than the XNORT. With the simplifying assumption that the output load is large (which lets us forget about differences in intrinsic capacitance), we can confidently assert that the XNORT will on average consume more dynamic power.

The transition probability of a two-input XOR is 0.25, which is slightly more than the XNORT. Therefore, we would expect the XNORT to consume less power, on average.

P(F:0 \rightarrow 1) = 0.23
4C  The path branching effort (product of stage branching efforts, which are the ratios of total driven capacitance to capacitance driven on the path) is:

\[ B_{path} = 1 \cdot 3 \cdot 1 \cdot 2 \cdot 1 = 6 \]

The path electrical effort (ratio of output capacitance to input capacitance) is:

\[ FO_{path} = C_L/C_{in} = 18\text{fF}/3\text{fF} = 6 \]

The path logical effort (product of stage logical efforts), using results from both the lectures and earlier in this problem, is:

\[ LE_{path} = LE_{inv} \cdot LE_{xnort,a} \cdot LE_{nand} \cdot LE_{xnort,b} \cdot LE_{nor} = 1 \cdot 4/3 \cdot 4/3 \cdot 2 \cdot 5/3 = 160/27 \]

The total path effort is then

\[ PE = LE_{path} \cdot B_{path} \cdot FO_{path} = 160/27 \cdot 6 \cdot 6 = 160 \cdot 4/3 \]

The optimum effort per stage for this five-stage path is

\[ SE^* = PE^{1/5} \approx 2.92 \]

4D  The effort for the stage is

\[ SE^* = b \cdot LE \cdot FO \Rightarrow C_{in} = LE \cdot C_{out} \cdot b / SE^* \]

Input capacitance of the NOR gate (last gate in the path) is:

\[ z = b \cdot LE_{nor} \cdot C_L / SE^* \approx 1 \cdot (5/3) \cdot (2.92) \cdot 18\text{fF} \approx 10.3\text{fF} \]

The stage effort for the second XNORT is:

\[ SE^* \approx 2 \cdot LE_{xnort,b} \cdot 10.3\text{fF}/y \Rightarrow y = b \cdot 10.3\text{fF} \cdot LE_{xnort,b} / SE^* \approx 2 \cdot 10.3\text{fF} \cdot 2 / 2.92 \approx 14.1\text{fF}. \]

Fanout of the NAND gate is:

\[ FO = 14.1\text{fF}/x \Rightarrow x = b \cdot 14.1\text{fF} \cdot LE_{nand} / SE^* \approx 1 \cdot 14.1\text{fF} \cdot (4/3) / 2.92 \approx 6.4\text{fF} \]

Fanout (electrical effort) for the first XNORT is:

\[ FO = 6.4\text{fF}/w \Rightarrow w \approx 3 \cdot 6.4\text{fF} \cdot LE_{xnort,a} / SE^* = 19.2\text{fF} \cdot (4/3) / 2.92 \approx 8.8\text{fF} \]

As a check, we see that the first stage effort is

\[ SE^* = b \cdot LE_{inv} \cdot FO = 1 \cdot 1 \cdot 8.8\text{fF}/3\text{fF} \approx 2.93, \]

which closely matches our calculated optimum effort per stage.
Appendix:
Other Possible Implementations for Problem 1B: