EE141 – Fall 2005
Lecture 23

Timing

Announcements

- Cadence help in labs this week
  - Creating hierarchical schematic
  - Mon & Thu, Tue & Fri labs merged

- Full lab schedule next week
  - Layout, LVS etc.

- Homework 9 due on Tue, Nov 29, 5pm
Today’s Lecture

- Sequential Circuits (Cont.)
- Timing

Sequential Logic
Other Latches/Registers: C²MOS

Keepers can be added to staticize

Other Latches/Registers: TSPC

Positive latch (transparent when CLK= 1)  Negative latch (transparent when CLK= 0)
Including Logic in TSPC

Example: logic inside the latch

AND latch

TSPC Register
Pulse-Triggered Latches

Ways to design an edge-triggered sequential cell:

Master-Slave Latches

Pulse-Triggered Latch

Pulsed Latches

(a) register

(b) glitch generation

(c) glitch clock
Pulsed Latches

Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7:

HLFF Timing
Other Sequential Circuits

- Schmitt Trigger
- Monostable Multivibrators
- Astable Multivibrators
**Schmitt Trigger**

- VTC with hysteresis
- Restores signal slopes

**Noise Suppression using Schmitt Trigger**
CMOS Schmitt Trigger

The effect of varying the ratio of the PMOS device $M_4$. The width is $k*0.5\,\mu\text{m}$.

Schmitt Trigger: Simulated VTC

The effect of varying the ratio of the PMOS device $M_4$. The width is $k*0.5\,\mu\text{m}$.
CMOS Schmitt Trigger (2)

Multivibrator Circuits

- **Bistable Multivibrator**
  - flip-flop, Schmitt Trigger

- **Monostable Multivibrator**
  - one-shot

- **Astable Multivibrator**
  - oscillator
Transition-Triggered Monostable

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<thead>
<tr>
<th>In</th>
<th>Out</th>
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<tbody>
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<td></td>
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Monostable Triggered (RC-based)

(a) Trigger circuit.

(b) Waveforms.
Astable Multivibrators (Oscillators)

Ring Oscillator

simulated response of 5-stage oscillator

Relaxation Oscillator

\[ T = 2(\log_3) \cdot RC \]
Voltage Controlled Oscillator (VCO)

Schmitt Trigger restores signal slopes

Current starved inverter

propagation delay as a function of control voltage

Timing
Outline

- **Timing parameters**
- Clock nonidealities (skew and jitter)
- Impact of Clk skew on timing
- Impact of Clk jitter on timing
- Flip-flop- vs. Latch-based timing
- Clock distribution

Synchronous Timing
**Datapath and Timing Parameters**

\[ t_{C - q}, t_{C - q, cd}, t_{su}, t_{hold}, t_{logic}, t_{logic, cd} \]

*R1 and R2 can be latches or flip-flops*

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**Latch Parameters**

\( \text{Delays can be different for rising and falling data transitions} \)
Flip-Flop Parameters

Delays can be different for rising and falling data transitions

Timing Constraints (Cycle Time and Race Margin)

Cycle time: $T_{Clk} > t_{c-q} + t_{logic} + t_{su}$

Race margin: $t_{hold} < t_{c-q,cd} + t_{logic,cd}$
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Clock Nonidealities

- **Clock skew**
  - Spatial variation in temporally equivalent clock edges; deterministic + random, $t_{SK}$

- **Clock jitter**
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
  - Cycle-to-cycle (short-term) $t_{JS}$
  - Long term $t_{JL}$

- Variation of the pulse width
  - for level sensitive clocking
Clock Skew and Jitter

- Both skew and jitter affect the effective cycle time
- Only skew affects the race margin

Clock Skew

- Earliest occurrence of Clk edge: Nominal - $T_{sk}/2$
- Latest occurrence of Clk edge: Nominal + $T_{sk}/2$
- Insertion delay: $T_{sk}$
- Max Clk skew

# of registers

Clk delay

Earliest occurrence of Clk edge

Latest occurrence of Clk edge

Nominal - $T_{sk}/2$

Nominal + $T_{sk}/2$

Insertion delay

Max Clk skew
Sources of Skew and Jitter

Positive Skew

Launching edge arrives before the receiving edge
Negative Skew

Receiving edge arrives before the launching edge

Positive and Negative Skew

(a) Positive skew

(b) Negative skew
Outline

- Timing parameters
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  - Impact of Clk skew on timing
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Timing Constraints

\[ Cycle\ time: \ T_{C_{lk}} > t_{c-q} + t_{\text{logic}} + t_{su} \]
\[ Race\ margin: \ t_{\text{hold}} < t_{c-q,cd} + t_{\text{logic,cd}} \]
**Impact of Clock Skew on Timing: Cycle Time (Long Path)**

\[ t_{c-q} + t_{\text{logic}} + t_{su} < T_{\text{Clk}} + \delta \]

\[ T_{\text{Clk}} > t_{c-q} + t_{\text{logic}} + t_{su} - \delta \]

**Impact of Clock Skew on Timing: Race Margin (Short Path)**

\[ t_{c-q,cd} + t_{\text{logic,cd}} > t_{\text{hold}} + \delta \]

\[ t_{\text{hold}} + \delta < t_{c-q,cd} + t_{\text{logic,cd}} \]
Impact of Clock Skew on Timing

Positive skew improves performance

\[ T_{\text{Clk}} > t_{c-q} + t_{\text{logic}} + t_{su} - \delta \]

Negative skew improves race margin

\[ t_{\text{hold}} + \delta < t_{c-q,cd} + t_{\text{logic,cd}} \]

Worst-case |\( \delta \)| really matters

How to Counter Clock Skew?

Clock Distribution

Positive Skew

Negative Skew

In \rightarrow Out
Outline

- Timing parameters
- Clock nonidealities (skew and jitter)
- Impact of Clk skew on timing
- **Impact of Clk jitter on timing**
- Flip-flop- vs. Latch-based timing
- Clock distribution

Impact of Clock Jitter

![Impact of Clock Jitter Diagram](image-url)
Impact of Clock Jitter on Timing: Cycle Time (Late-Early Problem)

\[ t_{c-q} + t_{\text{logic}} + t_{su} < T_{Clk} - t_{\text{jitter}} - t_{\text{jitter}} \]

\[ T_{Clk} > t_{c-q} + t_{\text{logic}} + t_{su} + 2t_{\text{jitter}} \]

Impact of Clock Jitter on Timing

Negative impact on cycle time

\[ T_{Clk} > t_{c-q} + t_{\text{logic}} + t_{su} + 2t_{\text{jitter}} \]

No direct effect on race immunity (same Clk edge)

Jitter reduces performance
Combined Impact of Clock Jitter and Clock Skew

Impact of Clock Skew and Jitter: Cycle Time (Late-Early Problem)

\[ t_{c-q} + t_{\text{logic}} + t_{su} < T_{\text{Clk}} - t_{\text{jitter}} - t_{\text{jitter}} + \delta \]

\[ T_{\text{Clk}} > t_{c-q} + t_{\text{logic}} + t_{su} - \delta + 2 t_{\text{jitter}} \]
Impact of Clock Skew and Jitter: Race Margin (Early-Late Problem)

- **Earliest** point of launching

Data must not arrive before this time

- **Latest** arrival of next cycle

$\delta$

Nominal clock edge

$t_{c-q,cd} + t_{logic,cd} - t_{jitter} > t_{hold} + t_{jitter} + \delta$

$t_{hold} + 2 t_{jitter} + \delta < t_{c-q,cd} + t_{logic,cd}$

Combined Impact of Clock Skew and Jitter on Timing

- **Cycle time**
  
  $T_{Clk} > t_{c-q} + t_{logic} + t_{su} - \delta + 2 t_{jitter}$

  - Positive skew improves performance
  - Negative skew reduces performance
  - Jitter reduces performance

- **Race Margin**
  
  $t_{hold} + 2 t_{jitter} + \delta < t_{c-q,cd} + t_{logic,cd}$

  - Skew reduces race margin
  - Jitter reduces acceptable skew
Next Lecture

- Timing (Cont.)
- Clock Distribution
- Interconnect