EE141 – Fall 2005
Lecture 24

Clock Distribution, Interconnect

Administrative Stuff

- Homework 9 due today 5pm

- Project presentations next Tuesday
  - 9:00-12:00 (476 Cory), 2:00-5:00 (400 Cory)
  - Sign-up for time-slot (sign-up sheet in 353 Cory)
  - Presentation template on web-site
Class Material

- Today’s lecture
  - Timing in presence of clock non-idealities
  - Clock distribution
  - Interconnect optimization

Impact of Clock Skew on Timing

Positive skew improves performance

\[ T_{C\text{l}k} > t_{c-q} + t_{\text{logic}} + t_{su} - \delta \]

Negative skew improves race margin

\[ t_{\text{hold}} + \delta < t_{c-q,cd} + t_{\text{logic,cd}} \]

Worst-case \(|\delta|\) really matters
Outline

- Timing parameters
- Clock nonidealities (skew and jitter)
- Impact of Clk skew on timing
- **Impact of Clk jitter on timing**
- Flip-flop- vs. Latch-based timing
- Clock distribution

Impact of Clock Jitter
Impact of Clock Jitter on Timing: Cycle Time (Late-Early Problem)

$$t_{c-q} + t_{\text{logic}} + t_{\text{su}} < T_{\text{Clk}} - t_{\text{jitter}} - t_{\text{jitter}}$$

$$T_{\text{Clk}} > t_{c-q} + t_{\text{logic}} + t_{\text{su}} + 2t_{\text{jitter}}$$

Impact of Clock Jitter on Timing

Negative impact on cycle time

$$T_{\text{Clk}} > t_{c-q} + t_{\text{logic}} + t_{\text{su}} + 2t_{\text{jitter}}$$

No direct effect on race immunity (same Clk edge)

**Jitter reduces performance**
Combined Impact of Clock Jitter and Clock Skew

Impact of Clock Skew and Jitter: Cycle Time (Late-Early Problem)

\[ t_{c-q} + t_{\text{logic}} + t_{su} < T_{\text{Clk}} - t_{jitter} - t_{jitter} + \delta \]

\[ T_{\text{Clk}} > t_{c-q} + t_{\text{logic}} + t_{su} - \delta + 2t_{jitter} \]

Latest point of launching

Earliest arrival of next cycle
Impact of Clock Skew and Jitter: Race Margin (Early-Late Problem)

\[ T_{\text{Clk}} > t_{c-q} + t_{\text{logic}} + t_{\text{su}} - \delta + 2t_{\text{jitter}} \]

- Positive skew improves performance
- Negative skew reduces performance
- Jitter reduces performance

- Race Margin
  \[ t_{\text{hold}} + 2t_{\text{jitter}} + \delta < t_{c-q,cd} + t_{\text{logic,cd}} \]

- Skew reduces race margin
- Jitter reduces acceptable skew
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Flip-Flop – Based Timing

[Horowitz96]
Flip-Flops and Dynamic Logic

Flip-flops are used only with static logic

Latch Timing

When data arrives to transparent latch
Latch is a ‘soft’ barrier

When data arrives to closed latch
Data has to be ‘re-launched’
Latch Timing (Cont.)

Latch-Based Design

L1 latch is transparent when $\Phi = 1$

L2 latch is transparent when $\Phi = 0$
Latch-Based Timing

Can tolerate skew!

Outline

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Clock Distribution

H-tree

Clock is distributed in a tree-like fashion

Clock Distribution

H-Tree Network

Observe: Only Relative Skew is Important
More Realistic H-Tree

[Restle98]

Clock Network with Distributed Buffering

Reduces absolute delay, and makes Power-Down easier
Sensitive to variations in Buffer Delay
The Grid System

• No RC-matching
• Large power

Example: Dec Alpha 21164

❖ Clock Frequency: 300 MHz, 9.3 Million Transistors
❖ Total Clock Load: 3.75 nF
❖ Power in Clock Distribution Network: 20 W (out of 50 W)
❖ Uses Two Level Clock Distribution:
  • Single 6-stage driver at center of chip
  • Secondary buffers drive left and right side
  • Clock grid in Metal-3 and Metal-4
  • Total driver size: 58 cm!
21164 Clocking (EV5), 1995

- Single-phase clocking
- 2 distributed driver channels
  - Reduced RC delay/skew
  - Improved thermal distribution
  - 3.75 nF clock load
  - 58 cm final driver width
- Local inverters for latching
- Conditional clocks in caches to reduce power
- More complex race checking
- Device variation

Clock waveform

Location of clock driver on die

Clock Drivers
**EV6 (Alpha 21264) Clocking**

600 MHz, 0.35\(\mu\)m CMOS, 1998

- Multiple conditional buffered clocks
  - 2.8 nF clock load
  - 40 cm final driver width
- Reduced load/skew
- Reduced thermal issues
- Multiple clocks complicate race checking

Global clock waveform

- \(t_{\text{rise}} = 0.15\text{ns}\)
- \(t_{\text{cycle}} = 1.67\text{ns}\)
- \(t_{\text{skew}} = 50\text{ps}\)
21264 Clocking

GCLK Skew
(at Vdd/2 Crossings)

GCLK Rise Times
(20% to 80% Extrapolated to 0% to 100%)

EV6 Clock Results
EV7 Clock Hierarchy, 2002

152 million transistors, 15/137 logic/memory

Active Skew Management and Multiple Clock Domains

+ widely dispersed drivers
+ DLLs compensate static and low-frequency variation
+ divides design and verification effort
- DLL design and verification is added work
+ tailored clocks

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Alpha Processors Case Study

- EV4 (21064) 0.75µm, 200 MHz ~ 1992
  - Single global clock driver, 5 levels of buffering
    - 35 cm driver, 3.25 nF, 40% power
- EV5 (21164) 0.5µm, 300 MHz ~ 1995
  - One central, two side clock drivers
    - 58 cm driver, 3.75 nF, 40% power
- EV6 (21264) 0.35µm, 600 MHz ~ 1998
  - Clock grid, 4 window panes, hierarchical, gated clock domains
    - 40 cm driver, 2.8 nF
- EV7 0.18µm, 1.2 GHz ~ 2002
  - Multiple clock domains, DLLs
Self-Timed and Asynchronous Design

Functions of clock in synchronous design
1) Acts as completion signal
2) Ensures the correct ordering of events

Truly asynchronous design
1) Completion is ensured by careful timing analysis
2) Ordering of events is implicit in logic

Self-timed design
1) Completion ensured by completion signal
2) Ordering imposed by handshaking protocol

Interconnect Issues
Impact of Interconnect Parasitics

- Reduce Robustness
- Affect Performance

Classes of Parasitics

- Capacitive
- Resistive
- Inductive

INTERCONNECT:

Dealing with Capacitance
**Capacitive Cross Talk: Dynamic Node**

\[
\Delta V_y = \frac{C_{xy}}{C_y + C_{xy}} \Delta V_x
\]

3 x 1 \( \mu \)m overlap: 0.19 V disturbance

**Capacitive Cross Talk Driven Node**

\[
\tau_{xy} = \tau_y (C_{xy} + C_y)
\]

Keep time-constant smaller than rise time
Dealing with Capacitive Cross Talk

- Avoid floating nodes
- Protect sensitive nodes
- Make rise and fall times as large as possible
- Differential signaling
- Do not run wires together for a long distance
- Use shielding wires
- Use shielding layers

Delay Degradation

- Impact of neighboring signal activity on switching delay
- When neighboring lines switch in opposite direction of victim line, delay increases

**Miller Effect**

- Both terminals of capacitor are switched in opposite directions \((0 \rightarrow V_{dd}, V_{dd} \rightarrow 0)\)
- Effective voltage is doubled and additional charge is needed (from \(Q=CV\))
Impact of Cross Talk on Delay

<table>
<thead>
<tr>
<th>bit k – 1</th>
<th>bit k</th>
<th>bit k + 1</th>
<th>Delay factor g</th>
</tr>
</thead>
<tbody>
<tr>
<td>↑</td>
<td>↑</td>
<td>↑</td>
<td>1</td>
</tr>
<tr>
<td>↑</td>
<td>↑</td>
<td>—</td>
<td>1 + r</td>
</tr>
<tr>
<td>↑</td>
<td>↑</td>
<td>↓</td>
<td>1 + 2r</td>
</tr>
<tr>
<td>—</td>
<td>↑</td>
<td>—</td>
<td>1 + 2r</td>
</tr>
<tr>
<td>—</td>
<td>↑</td>
<td>↓</td>
<td>1 + 3r</td>
</tr>
<tr>
<td>↓</td>
<td>↑</td>
<td>↓</td>
<td>1 + 4r</td>
</tr>
</tbody>
</table>

r is ratio between capacitance to GND and to neighbor

Interconnect Projections: Low-k Dielectric

- Both *delay and power are reduced* by dropping interconnect capacitance
- Types of low-k materials include: inorganic (SiO₂), organic (Polyamides) and aerogels (ultra low-k)
- The numbers below are on the conservative side of the NRTS roadmap

<table>
<thead>
<tr>
<th>Generation</th>
<th>0.25 µm</th>
<th>0.18 µm</th>
<th>0.13 µm</th>
<th>0.1 µm</th>
<th>0.07 µm</th>
<th>0.05 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Constant</td>
<td>3.3</td>
<td>2.7</td>
<td>2.3</td>
<td>2.0</td>
<td>1.8</td>
<td>1.5</td>
</tr>
</tbody>
</table>
How to Battle Capacitive Crosstalk

- Avoid large crosstalk Cs
- Avoid floating nodes
- Isolate sensitive nodes
- Control rise/fall times
- Shield!
- Differential signaling

Driving Large Capacitances

\[ t_p = \frac{C_L V_{swing}}{I_{av}} \]

- Transistor Sizing
- Cascaded Buffers
Using Cascaded Buffers

![Cascaded Buffers Diagram]

\[ C_L = 20 \, pF \]

- 0.25 \( \mu \)m process \( F = CL/Cin = 8000 \)
- \( Cin = 2.5 \, fF \) \( fopt = 3.6 \) \( N = 7 \)
- \( tp0 = 30 \, ps \) \( tp = 0.76 \, ns \)

(See Chapter 5)

Output Driver Design

Trade off Performance for Area and Energy

Given \( t_{pmax} \) find \( N \) and \( f \)

- **Area**
  \[ A_{driver} = \left(1 + f + f^2 + \ldots + f^{N-1}\right) \cdot A_{min} = \frac{f^N - 1}{f - 1} A_{min} = \frac{F - 1}{f - 1} A_{min} \]

- **Energy**
  \[ E_{driver} = \left(1 + f + f^2 + \ldots + f^{N-1}\right) \cdot C LV^2_D = \frac{F - 1}{f - 1} C LV^2_D \approx \frac{C_L}{f - 1} V^2_D \]
Delay as a Function of F and N

\[
\frac{t_p}{t_p^0} \quad F = 10,000 \quad F = 1000 \quad F = 100
\]

Number of buffer stages \( N \)

Output Driver Design

0.25 \( \mu \)m process, \( C_L = 20 \) pF

Transistor Sizes for optimally-sized cascaded buffer \( t_p = 0.76 \) ns

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_e (\mu m) )</td>
<td>0.375</td>
<td>1.35</td>
<td>4.86</td>
<td>17.5</td>
<td>63</td>
<td>226.8</td>
<td>816.5</td>
</tr>
<tr>
<td>( W_p (\mu m) )</td>
<td>0.71</td>
<td>2.56</td>
<td>9.2</td>
<td>33.1</td>
<td>119.2</td>
<td>429.3</td>
<td>1545.5</td>
</tr>
</tbody>
</table>

Transistor Sizes of redesigned cascaded buffer \( t_p = 1.8 \) ns

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_e (\mu m) )</td>
<td>0.375</td>
<td>7.5</td>
<td>130</td>
</tr>
<tr>
<td>( W_p (\mu m) )</td>
<td>0.71</td>
<td>14.4</td>
<td>284</td>
</tr>
</tbody>
</table>

7.5x smaller area
ESD Protection

- When a chip is connected to a board, there is unknown (potentially large) static voltage difference
- Equalizing potentials requires (large) charge flow through the pads
- Diodes sink this charge into the substrate – need guard rings to pick it up.
**ESD Protection**

![ESD Protection Diagram](image)

**Chip Packaging**

- Bond wires (~25µm) are used to connect the package to the chip
- Pads are arranged in a frame around the chip
- Pads are relatively large (~100µm in 0.25µm technology), with large pitch (100µm)
- Many chips areas are ‘pad limited’
Pad Frame

Layout

Die Photo

Next Lecture

- Power Distribution

- Memory