EE141 - Fall 2005
Lecture 26

Memory (Cont.)
Perspectives

Administrative Stuff

- Homework 10 posted – just for practice
  - No need to turn in
- Office hours next week, schedule TBD.
- HKN review today. Your feedback is important!
- Final covers all material covered in class.
  Precise overview to be posted on web-site.
- Review session schedule TBD.
**Project 2 – Summary**

- Variety of topologies and circuit styles
  - Most projects focused on mix of static logic families

- Some very impressive presentations
  - Refer to examples on web-site

- Grades
  - Mean: 79.3
  - Median: 78.9 (3.868, static)
  - Sigma: 19
  - Max: 110 (0.944, dynamic; 1.316, static)

---

**Sizing Optimization**

\[
\begin{align*}
LE &= 1 \times 1 \times \frac{4}{3} \times 2 \times 1 = \frac{8}{3} \\
FO &= 16 \\
\text{Branching : 4} \\
P &= \left( \frac{8}{3} \times 16 \times 4 \right)^{\frac{1}{3}} = 2.8 \\
\text{Size: } x &= 1.93 \\
y &= 4.08 \\
z &= 5.70 \\
\end{align*}
\]
**Layout Techniques**

- Size: 1265.22 µm²
  
  \[(33.00\text{µm} \times 38.34\text{µm})\]

- Critical Path drawn in arrow

- Aspect Ratio = 1.162

- Routing
  
  - Metal 1
    - Horizontal Line
    - VDD, GND
  
  - Metal 2:
    - Vertical Line
  
  - Metal 3:
    - Clock Signals

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**Memory**
## Semiconductor Memory Classification

<table>
<thead>
<tr>
<th>Read-Write Memory</th>
<th>Non-Volatile Read-Write Memory</th>
<th>Read-Only Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random Access</td>
<td>Non-Random Access</td>
<td></td>
</tr>
<tr>
<td>SRAM</td>
<td>FIFO</td>
<td>EPROM</td>
</tr>
<tr>
<td>DRAM</td>
<td>LIFO</td>
<td>E²PROM</td>
</tr>
<tr>
<td></td>
<td>Shift Register</td>
<td>FLASH</td>
</tr>
<tr>
<td></td>
<td>CAM</td>
<td>Mask-Programmed</td>
</tr>
<tr>
<td></td>
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<td>Programmable (PROM)</td>
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## Read-Only Memory Cells

- **Diode ROM**
- **MOS ROM 1**
- **MOS ROM 2**
MOS NOR ROM

MOS NOR ROM Layout

Programming using the Active Layer Only

Cell (9.5λ x 7λ)

Polysilicon
Metal1
Diffusion
Metal1 on Diffusion
MOS NOR ROM Layout

Cell (11λ x 7λ)

Programming using the Contact Layer Only

- Polysilicon
- Metal1
- Diffusion
- Metal1 on Diffusion

All word lines high by default with exception of selected row

- Pull-up devices

MOS NAND ROM

- V_{DD}

All word lines high by default with exception of selected row
No contact to VDD or GND necessary; drastically reduced cell size
Loss in performance compared to NOR ROM

Programming using the Metal-1 Layer Only

MOS NAND ROM Layout

NAND ROM Layout

Programming using Implants Only
PMOS precharge device can be made as large as necessary, but clock driver becomes harder to design.

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<td>SRAM DRAM</td>
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<td>E²PROM</td>
</tr>
<tr>
<td></td>
<td>LIFO</td>
<td>FLASH</td>
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Non-Volatile Memories
The Floating-gate transistor (FAMOS)

Floating-gate Transistor Programming

Avalanche injection
Removing programming voltage leaves charge trapped
Programming results in higher $V_T$. 
**FLOTOX EEPROM**

FLOTOX transistor

- Floating gate
- Source
- Substrate
- Drain
- Gate
- 20–30 nm

Fowler-Nordheim I-V characteristic

I

-10 V

V_{GD}

10 V

**EEPROM Cell**

Absolute threshold control is hard
Unprogrammed transistor might be depletion
⇒ 2 transistor cell
Cross Sections of NVM Cells

Read-Write Memories (RAM)

- **Static (SRAM)**
  - Data stored as long as supply is applied
  - Large (6 transistors/cell)
  - Fast
  - Differential

- **Dynamic (DRAM)**
  - Periodic refresh required
  - Small (1-3 transistors/cell)
  - Slower
  - Single ended
6-Transistor CMOS SRAM Cell

CMOS SRAM Analysis (Read)

\[ k_{n,M5}(V_{DD} - \Delta V - V_{TH}) V_{DSATn} - \frac{V_{DSATn}^2}{2} = k_{n,M1}(V_{DD} - V_{TH}) \Delta V - \frac{\Delta V^2}{2} \]

\[ \Delta V = \frac{V_{DSATn} + CR(V_{DD} - V_{TH}) - \frac{\sqrt{V_{DSATn}^2(1 + CR)}}{CR} + CR^2(V_{DD} - V_{TH})^2}{CR} \]
CMOS SRAM Analysis (Read)

\[
CR = \frac{W_1/L_1}{W_3/L_3}
\]

CMOS SRAM Analysis (Write)

\[
k_{n,M6}(V_{DD} - V_{Ta})V_Q - \frac{V_Q^2}{2} = k_{p,M4}(V_{DD} - |V_{Tp}|)V_{DSATp} - \frac{V_{DSATp}^2}{2}
\]

\[
V_Q = V_{DD} - V_{Ta} - \sqrt{(V_{DD} - V_{Ta})^2 - \frac{2}{i_a}V_{PPR}(V_{DD} - |V_{Tb}|)V_{DSATp} - \frac{V_{DSATp}^2}{2}}
\]
CMOS SRAM Analysis (Write)

![Graph showing cell voltage vs. pull-up ratio]

6T-SRAM Layout

![Diagram of 6T-SRAM layout with transistors and nodes labeled]

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Resistive Load SRAM Cell

Static power dissipation -- Want $R_L$ large
Bit lines precharged to $V_{DD}$ to address $t_p$ problem

3-Transistor DRAM Cell

No constraints on device ratios
Reads are non-destructive
Value stored at node $X$ when writing a “1” = $V_{WWL} - V_{Tn}$
### 3T DRAM Layout

**Write**: CS is charged or discharged by asserting WL and BL.

**Read**: Charge redistribution takes place between bit line and storage capacitance. Voltage swing is small; typically around 250 mV.

### 1-Transistor DRAM Cell

**Write**: $C_S$ is charged or discharged by asserting WL and BL.

**Read**: Charge redistribution takes place between bit line and storage capacitance.

$$
\Delta V = V_{BL} - V_{PRE} = V_{BIT} - V_{PRE} \frac{C_S}{C_S + C_{BL}}
$$

Voltage swing is small; typically around 250 mV.
1T DRAM Cell

Cross-section

Uses Polysilicon-Diffusion Capacitance
Expensive in Area

Micrograph of 1T DRAM
Advanced 1T DRAM Cells

- Trench Cell
- Stacked-capacitor Cell

Perspectives
EE141 Summary

- Digital circuit designers will have jobs in 2010+
- Major challenges
  - Cost
  - Power consumption
  - Robustness
  - Complexity
- Some new circuit solutions and design methodologies are coming

Technology Scaling

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</thead>
<tbody>
<tr>
<td>Technology Node (nm)</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
<td>16</td>
<td>11</td>
<td>8</td>
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<tr>
<td>Integration Capacity (BT)</td>
<td>0.5</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>8</td>
<td>16</td>
<td>32</td>
<td>64</td>
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<tr>
<td>Delay = CV/I scaling</td>
<td>0.7</td>
<td>~0.7</td>
<td>&gt;0.7</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Energy/Logic Op scaling</td>
<td>&gt;0.35</td>
<td>&gt;0.5</td>
<td>&gt;0.5</td>
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<tr>
<td>Bulk Planar CMOS</td>
<td>High Probability</td>
<td>Low Probability</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Alternate, 3G etc</td>
<td>Low Probability</td>
<td>High Probability</td>
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<tr>
<td>Variability</td>
<td>Medium</td>
<td>High</td>
<td>Very High</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>ILD (K)</td>
<td>~3</td>
<td>&lt;3</td>
<td>Reduce slowly towards 2-2.5</td>
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<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>RC Delay</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Metal Layers</td>
<td>6-7</td>
<td>7-8</td>
<td>8-9</td>
<td>0.5 to 1 layer per generation</td>
<td></td>
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</tr>
</tbody>
</table>

 Courtesy: R. Krishnamurthy (Intel)
Research Roadmap

Device Evolution

Robert Chau, Intel, ICSICT 2004
25nm FinFET

25 nm MOS transistor (Folded Channel)

Cost

- Mask cost in 90nm technology is over $1M
- Bugs are very expensive
- Design effort increases in DSM
- Cost of new tools
- Non-recurring costs dominate the price effectiveness of low-volume ASICs
- Need to have a product that can fit multiple applications, customers (flexibility)
Power has become a Problem

Source: S. Borkar (Intel)

The Productivity Gap

Source: Sematech

Complexity outpaces design productivity
Some FPGA Examples

Xilinx Spartan-3

Xilinx IQ

The Architectural Tradeoff Game
The Challenge of the Next Decade

- The Deep Sub-Micron (DSM) Effect

\[ \propto \text{DSM} \quad \propto \frac{1}{\text{DSM}} \]

“Microscopic Problems”
- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock Distribution

“Macroscopic Issues”
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

...and there’s a lot of them!

Everything looks a little different