Announcements

- Hardware lab this week
  - Lab 4, 5 reports due this week
- Homework #6 due today
- Homework #7 due next Tuesday
- Project phase one in lab next week
Class Material

- Last lecture
  - Design for speed
  - Logical effort
- Today’s lecture
  - SRAM
  - Register files
- Reading (Chapters 12, 6)
Array-Structured Memory Architecture

Semiconductor Memory Classification

<table>
<thead>
<tr>
<th>Read-Write Memory</th>
<th>Non-Volatile Read-Write Memory</th>
<th>Read-Only Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Random Access</strong></td>
<td><strong>Non-Random Access</strong></td>
<td><strong>EPROM</strong></td>
</tr>
<tr>
<td>SRAM</td>
<td>FIFO</td>
<td><strong>E²PROM</strong></td>
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<tr>
<td>DRAM</td>
<td>LIFO</td>
<td><strong>FLASH</strong></td>
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<td></td>
<td>Shift Register</td>
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<td></td>
<td>CAM</td>
<td><strong>Mask-Programmed</strong></td>
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<td></td>
<td></td>
<td><strong>Programmable (PROM)</strong></td>
</tr>
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</table>
Read-Write Memories (RAM)

- **STATIC (SRAM)**
  - Data stored as long as supply is applied
  - Large (6 transistors/cell)
  - Fast
  - Differential

- **DYNAMIC (DRAM)**
  - Periodic refresh required
  - Small (1-3 transistors/cell)
  - Slower
  - Single Ended

Positive Feedback: Bi-Stability

\[ V_{o1} \quad V_{o2} \]

\[ V_{i1} = V_{o2} \quad V_{i2} = V_{o1} \]

\[ V_{o1} = V_{i2} \quad V_{o2} = V_{i1} \]
**Meta-Stability**

Gain should be larger than 1 in the transition region

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**Writing into a Cross-Coupled Pair**

Can implement as a transmission gate as well
Access transistor must be able to overpower the feedback
\[ k_1 \frac{w_a}{L} \left( (v_{in}-v_b) - \frac{v_a^2}{2} \right) = k_2 \frac{w_b}{L} \left( v_{in} - v_c^2 \right) \]
**Memory Cell**

Complementary data values are written (read) from two sides

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**6-transistor CMOS SRAM Cell**
SRAM Operation

Write

Hold

SRAM Operation

Read

Reading the cell should not destroy the stored value
CMOS SRAM Analysis (Read)

\[
\Delta V = \frac{V_{\text{DSAT}_4} \cdot CR (V_{\text{DD}} - V_{\text{TH}}) - V_{\text{DSAT}_3}^2 (1 + CR) + CR^2 (V_{\text{DD}} - V_{\text{TH}})^2}{CR}
\]

\[
k_{\text{M}5} (V_{\text{DD}} - \Delta V - V_{\text{TH}}) V_{\text{DSAT}_3} - \frac{V_{\text{DSAT}_3}^2}{2} = k_{\text{M}1} (V_{\text{DD}} - V_{\text{TH}}) \Delta V - \frac{\Delta V^2}{2}
\]
CMOS SRAM Analysis (Write)

\[ k_{x, M1} \left( V_{DD} - V_Tp \right) V_0 - \frac{V_D^2}{2} = k_{x, M1} \left( V_{DD} - |V_Tp| \right) V_{Dsat} - \frac{V_D^2}{2} \]

\[ V_0 = V_{DD} - V_{Tn} - \sqrt{\left( V_{DD} - V_{Tn} \right)^2 - \frac{\mu \cdot C \cdot V_{DD}}{W} \left( V_{DD} - |V_Tp| \right) V_{Dsat} - \frac{V_D^2}{2}}. \]

\[ PR = \frac{W}{L} \]

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CMOS SRAM Analysis (Write)

Cell voltage [V]

<table>
<thead>
<tr>
<th>Pull-up Ratio</th>
<th>0.5</th>
<th>0.4</th>
<th>0.3</th>
<th>0.2</th>
<th>0.1</th>
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<tbody>
<tr>
<td>0</td>
<td>0.0</td>
<td>0.1</td>
<td>0.2</td>
<td>0.3</td>
<td>0.4</td>
</tr>
<tr>
<td>0.5</td>
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<td>0.4</td>
<td>0.3</td>
<td>0.2</td>
<td>0.1</td>
</tr>
<tr>
<td>1</td>
<td>1.0</td>
<td>0.9</td>
<td>0.8</td>
<td>0.7</td>
<td>0.6</td>
</tr>
<tr>
<td>1.5</td>
<td>1.5</td>
<td>1.4</td>
<td>1.3</td>
<td>1.2</td>
<td>1.1</td>
</tr>
<tr>
<td>2</td>
<td>2.0</td>
<td>1.9</td>
<td>1.8</td>
<td>1.7</td>
<td>1.6</td>
</tr>
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</table>

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Read Static Noise Margin

Obtained by breaking the feedback between the inverters
6T-SRAM — Layout

- Compact cell
- Bitlines: M2
- Wordline: bootstrapped in M3

65nm SRAM

- ST/Philips/Motorola

Access Transistor

Pull down

Pull up
Register File

- Schematic very similar to SRAM cell
  - But layout different
  - Sizing different
- Needs multiple read/write ports
Register File

Single port

Two-port

Register file
Next Lecture

- Combinational logic
- Decoders