PROBLEM 1: Complex CMOS Gates

For this problem you should use the following parameters for the transistors.

**NMOS:**
- \( L = 100 \text{nm} \)
- \( V_{th} = 0.25 \text{V} \)
- \( \mu_n = 350 \text{ cm}^2/(\text{V} \cdot \text{s}) \)
- \( C_{ox} = 0.95 \text{ \mu F/cm}^2 \)
- \( \nu_{sat} = 1 \times 10^7 \text{ cm/s} \)
- \( \lambda = 0 \)

**PMOS:**
- \( L = 100 \text{nm} \)
- \( |V_{tp}| = 0.25 \text{V} \)
- \( \mu_p = 175 \text{ cm}^2/(\text{V} \cdot \text{s}) \)
- \( C_{ox} = 0.65 \text{ \mu F/cm}^2 \)
- \( \nu_{sat} = 1 \times 10^7 \text{ cm/s} \)
- \( \lambda = 0 \)

a) Implement the function \( F = AD(C + B) \). Assuming long-channel transistors, size the devices so that the worst-case drive resistance is the same as an inverter with \( W_N/L = 2 \) and \( W_P/L = 4 \).

b) Imagine that input "B" to the gate was always the last one to arrive, making the delay of the gate from B rising or falling to the output falling or rising critical. Please re-arrange the implementation of your gate so that the delay of the gate from B transitioning is minimized.

c) Draw a stick diagram of the gate you designed for part b) - you should minimize the diffusion breaks and use a single piece of poly for each input.

d) Now resize the gate to match the worst-case pull-up and pull-down resistances using the velocity saturated model. What is the LE from the B input?

e) Use SPICE to extract the LE from the B input for the gate with the sizing from part d). How does this compare with the result predicted from part d)?

PROBLEM 2: Bus of Signals

In this problem we will be looking at a bus of data signals that might exist in order to transfer data from one part of the chip to another. You should assume that the wires are 1mm long and implemented in M3 (which has a minimum width of 0.2\( \mu \)m, \( R_w = 0.075 \Omega/\square \)) and are running over active. You can also assume that there are no higher metal layers running above it and that the wires are layed out at the minimum allowed spacing. Use table 4-2, 4-3 in the text book to find the unit capacitance values.
a) What is the total resistance of each wire?

b) What is the total capacitance of each wire to ground? How about the total capacitance to each of its neighbors?

c) Assuming the bus has only 3 wires, what is worst case energy pulled out of the supply of the middle driver for one transition (you can ignore the capacitance that comes from transistors)? Under what condition pattern of inputs to the bus does this occur?

**Problem 3: Repeaters**

For this problem, use the following parameters for the wire: \( R = 0.075 \, \Omega/\square \), \( W = 0.2 \, \text{um} \), and \( C = 0.2 \, \text{fF/um} \) (this number includes the effects of both parallel plate and fringe capacitance). For the inverters you should assume that \( V_{\text{dd}} = 1.2 \, \text{V} \), \( C_{g} = 2 \, \text{fF/um} \), \( C_{d} = 1.6 \, \text{fF/um} \), \( R_{\text{nm}} = 10 \, \text{k}\Omega/\square \), and \( R_{\text{pm}} = 20 \, \text{k}\Omega/\square \). All of the inverters in Figure 1 are the same size as the first inverter.

![Figure 1](image)

a) Draw an RC model for the above circuit and calculate the delay from the input to \( V_{\text{out}} \). You should include slope effect – in other words, you can approximate the Elmore delay as being equal to just \( RC \) (instead of \( \ln(2)\times RC \)).

b) Now assume you have a wire with a total length of \( L \) and that this wire is broken into \( N \) repeated sections with identically sized inverters (where each inverter is a factor of \( S \) bigger than the inverters shown in Figure 2). How does delay depend on \( N \), inverter sizing \( S \), and wire length \( L \)?

c) What \( N \) and \( S \) minimize the delay for a given \( L \)?