PROBLEM 1: VTC

In this problem we will analyze the noise margins for a chain of identical gates, Figure 1(a). The VTC for these gates is piece-wise linear with six segments, where each segment is a straight line, as shown in Figure 1(b).

a) Add the DC voltage sources to Figure 1(a) that you would use for modeling noise coupling to the input and output of gate $M_2$. You should arrange these voltage sources so that they would both impact the noise margin in the same way (i.e., if the voltage source at the input decreases the noise margin, the voltage source at the output should also decrease the noise margin).

b) Determine the noise margins (as defined in lecture) for gate $M_2$ when noise couples only to its input. We want a numerical answer in Volts, not one based on just looking at the VTC.

c) Consider a gate $M_4$ that has a VTC as shown in Figure 1(c). Assuming that $VA<VB$ and $VC<VD$, define the relationships between $VA$, $VB$, $VC$ & $VD$ that would make $M_4$ digital.
d) Consider the cascade of gates $M_3$ and $M_4$, as shown in Figure 1(d), where $M_3$ is the gate from parts (a) & (b), and $M_4$ is the gate from part (c). If $V_A = 0.2V$, $V_B = 0.7V$ and $V_D = 1.2V$ (as shown in the figure), what is the range of values of $V_C$ for which the cascade is digital? As a part of your answer, sketch out the VTC of the cascade of $M_3$ and $M_4$.

PROBLEM 2: DELAY

Recall that we have defined the propagation delay $t_p$ as the time between the 50% transition points of the input and output waveforms. In this problem, we will explore how the way you set up a simulation can affect the results you measure. Please turn in a single spice deck that performs the simulations for parts b) through d). You can measure
the delays either by using .MEASURE statements in SPICE, or using WaveView. However, if you use WaveView you should include plots of your waveforms.

![Inverter Diagram](image)

(a) Create a SPICE subcircuit for the inverter shown above. Use the following line in your SPICE deck to obtain the correct NMOS and PMOS transistor models:

```
.LIB '/home/ff/ee141/MODELS/gpdk090_mos.sp' TT_s1v
```

To help get you started, we have provided the following example which demonstrates the creation and usage of subcircuits in SPICE. The following input creates an instance named X1 of the MYRC subcircuit, which consists of a 5kΩ resistor and 10fF capacitor in parallel.

```
X1 TOP BOTTOM MYRC
.SUBCKT MYRC A B
R1 A B 5k
C1 A B 10f
.ENDS
```

(b)
b) Measure the average propagation delay of an inverter driving four copies of itself (Fig. 2a). First apply a step input with a rise/fall time of 1 ns to the first inverter. Then, repeat this measurement with a rise/fall time of 1 ps. Note: Use the \textit{M (Multiply)} parameter in the subcircuit instantiation to replicate the inverter.

c) Now create a chain of four inverters, each with a fanout of 4 (Fig. 2b). Measure the average propagation delay of the second inverter in the chain when applying a step input to the first inverter. Is the delay from part b) or part c) more realistic in terms of what you might see on an actual IC? Explain the role of the first inverter in the chain.

d) Repeat part c) with the chain of four inverters, each with the fanout of 4 (Fig. 2c), but this time add a 10 fF capacitor (which could be from a wire) between the second and the third inverter. Compare this delay with the result from part c).

e) Now let’s use the circuit from Fig. 2d to see how connecting the capacitor in a different way may have more or less impact on the delay. Notice that the input to the lower inverter chain in the figure is complementary to the input given to the upper chain. In other words, when the input to the upper chain rises, the input to the lower chain falls (and vice versa).

What value of C do you need to use to make the delay of the circuit from Fig. 2d match the delay you measured in part d)? Why might this capacitor be larger or smaller than the 10fF used in part d)?

\textbf{PROBLEM 3: SWITCH MODEL}
In this problem, you should use the simple switch model for MOSFETs with the following characteristics: $|V_{TP}| = V_{dd}/3$, $V_{TN} = V_{dd}/3$

a) Sketch the VTC of the circuit shown in Figure 3(a) when $R = 2*R_{NMOS}$.

b) Sketch the VTC of the circuit shown in Figure 3(b) when $R_{PMOS} = 2*R_{NMOS}$.

c) For the circuit shown in Figure 3(c), consider the following scenario. $R_{PMOS} = 10*R_{NMOS}$. The inverter $M$ has an ideal VTC as shown in Fig. 3(d). $V(A)$ is held constant at $Vdd$, $V(OUT)$ is initially equal to $Vdd$, and $V(B)$ is initially equal to 0V. Sketch $V(OUT)$ vs. $V(B)$ with $V(B)$ swept from 0V to $Vdd$. In other words, you should assume that $V(B)$ starts at 0V and then plot what happens to $V(OUT)$ as you increase $V(B)$ up to $Vdd$. (The curve you are drawing is very much like a VTC, but is only valid when the input and output start in the given states.)

d) For part 3(c) if $R_{PMOS} = R_{NMOS}$, with all other conditions remaining the same, redraw $V(OUT)$ vs. $V(B)$ with $V(B)$ swept from 0V to $Vdd$. 

Figure 3