**How to Determine which is Drain/Source in Pass Transistor Logic**

![Circuit Diagrams](image)

Hopefully by now, you would recognize the above NMOS/PMOS configurations as pass transistor logic. In order to understanding the static behavior of the above, it is essential to recognize the location of the drain and source.

Consider Circuit (i), \( V_A = V_{dd} \). Assume initial conditions \( V_{in} = V_{out} = 0 \); Suppose further that and a step function is applied at \( V_{in} \):

- \( V_1 \) is forced by \( V_{in} \) to \( V_{dd} \).
- \( V_2 \) remains at 0V due to output capacitance.
- \( V_{12} > 0 \).
- Since a potential difference exists, we expect a drain current to flow from Node 1 to Node 2.
- We know that in a NMOS transistor, current flows from **Drain-to-Source**.

**Node 1: Drain**  
**Node 2: Source**

- \( V_{gs} = V_{dd} - V_2 \)

Now, with \( V_{out} = V_{OH} \) a negative step is applied at \( V_{in} \).
• \( V_1 \) is forced by \( V_{in} \) to 0.
• \( V_2 \) remains at \( V_{OH} \) due to output capacitance.
• \( V_{12} < 0 \).
• Since a potential difference exists, we expect a drain current to flow from Node 2 to Node 1.
• We know that in a NMOS transistor, current flows from **Drain-to-Source**.

**Node 2: Drain**
**Node 1: Source**

• \( V_{gs} = V_{dd} - V_1 \)

Repeat similar exercise for Circuit (ii) using \( V_A = 0 \) , and initial conditions \( V_{in} = V_{out} = V_{dd} \). Familiarize yourself with PMOS pass transistors. Remember that in the PMOS, current always flow from **Source-to-Drain**.

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