EECS 141: Spring 1999 - MIDTERM 1

Midterm Exam: Thursday, February 18
Open Book, Open Notes, Write directly on this exam.

CMOS Parameters:

\[ V_T(V) \quad k'(A/V^2) \]

NMOS 0.70 \quad 20 \times 10^{-6}
PMOS 0.70 \quad 8 \times 10^{-6}

Neglect Body Effect and Channel length Modulation unless specified otherwise.

PRINT Your Name.  

SIGN Your Name.

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I. (40 Points) Static Analysis

1.a. (20 Points) Set up an equation for $V_{\text{OUT}}$ and solve for $V_{\text{OUT}}$ to an accuracy of 0.2 volts when $V_A = 3V$ and $V_B = 5V$.

\[
I_n = \frac{A_n}{L_p} \left( \frac{W}{L} \right)_p \left[ (V_n - V_{n-1})V_{os} - \frac{V_{os}}{2} \right]
\]

\[
100 \mu A = \frac{(2)(3)}{2} \left[ (3-0.7)V_{os} - \frac{V_{os}}{2} \right]
\]

\[
V_{\text{OUT}} = \frac{100 \mu A}{(2)(3)} = \frac{100}{60} = 1.67 \text{ V}
\]

1.b. (20 Points) Find the minimum value of $(W/L)_p$ such that when $V_A = 5V$ and $V_B = 0V$, the output voltage (including the 100 $\mu A$ current) will be less than or equal to 1.5V. Note that both $V_A$ and $V_B$ have changed from part a.

\[
I_n = \frac{(2)(3)}{2} \left[ (5-0.7)(1.5) - \frac{1.5}{2} \right]
\]

\[
= (2)(3)(5.325) = 31.9 \text{ mA}
\]

\[
L \leq 5 \text{ mm}
\]

\[
21.55 = \Theta \left( \frac{W}{L} \right)_p \left[ (5-0.7)(3.5) - \frac{3.5}{2} \right] = \Theta \left( \frac{W}{L} \right)_p (8.5)
\]

\[
\left( \frac{W}{L} \right)_p = \frac{21.55}{\Theta (8.5)} = 3.07
\]
II. (40 Points) Transient Analysis of CMOS

\[ V DD \]

\[ V_{OUT} \]

\[ C_L = 5 \times 10^{-12} \text{ F} \]

II.a. (15 Points) Assuming the only capacitance present is \( C_L \), find the worst case propagation delay.

\[ T_{PLH} = (0.69) \left( \frac{20k + 30}{6} \right) (50 + 6) = 431 \text{ ps} \]

II.b. (15 Points) Using the \( C_{DBP} \) and \( C_{DBN} \) values given above and the \((W/L)\) sizes shown, find the total internal capacitance which has the possibility of changing voltage.

\[ \begin{align*}
N_{LM} &= 6 + 2 + 2 = 10 \text{ ns} \\
\mu & = 6 \text{ ns} \\
\gamma & = 2 \text{ ns} \\
C_{DBP} &= (4)(1.5) = 6 \text{ fF} \\
C_{DBN} &= (4)(1.5) = 6 \text{ fF} \\
C_{DB} &= C_{DBP} + C_{DBN} = 12 \text{ fF} \\
\text{Total Capacitance} &= 6 + 10 + 12 = 28 \text{ fF}
\end{align*} \]

II.c. (10 Points) Find the worst case propagation delay when both \( C_L \) and the \( C_{DB} \) internal capacitances are present.

\[ (0.69) \left[ \frac{30k + 30}{6} (50 + 10.5 + 6) \right] + \left( \frac{30}{4} \right) (6 \times 10^{-12}) = 169 \left[ 6 \times 10^{-5} + 2 \times 10^{-12} \right] + 10 \times 10^{-12} = 657 \text{ ps} \]
III. (40 Points) CCMOS and Standard Cells

III.a (15 Points) Sketch the circuit and find the logic function of the standard cells STICK Diagram.

\[ x = a + b \]
\[ F = de \]
\[ F = \overline{de} = d + \overline{e} = a + b + \overline{e} \]

III.b (25 Points) Design a standard cells STICKS diagram for \( F = abc + de + f \).
IV. (30 Points) Pass Transistor and Body Effect

IV.a. (15 Points) Find the logic function generated by the circuit below and explain how \( F \) is well defined for all possible input combinations.

\[ F = A \bar{b} \bar{c} \]

\( C = 0 \) Right Vertical Path Connects to Low \( \Rightarrow \)
All \( \bar{A} = 0 \) Well Defined

\( C \neq 0 \) \( \bar{B} = 0 \) Right Vertical Path Connects to Low \( \Rightarrow \)
2 Additional Cases Will Define Low

\( C \neq 0 \) \( B \neq 0 \) Horizontal Path Connects Value of \( A \)
So Last Two \( A = 1 \ A = 0 \) Well Defined

(15 Points) List 5 reasons why \( t_{PHL} \) and \( t_{PLH} \) can be unequal.

1) \( U_n \neq U_p \)
2) \( K_{ep} \neq K_{en} \) as \( v_{dd} \) goes \( V_{dd} \rightarrow V_{dd}^L \)
3) PMOS (P) can have a different vertical path
4) Internal distribution can flow along different SR and
5) Ratio logic has asymmetry in current

Statistical by design