Problem #1
Calculate the Elmore delay from node A to node B using the values for the resistors and capacitors given in the table below.

First, let’s label all the nodes:

Following the formula for Elmore delay in Chapter 4 of the book, (Equations 4.12 and 4.13), we first calculate the $R_{IB}$ for each node (results in table below).

<table>
<thead>
<tr>
<th></th>
<th>common resistance from A to Node and B</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{BB}$</td>
<td>1001.75</td>
</tr>
<tr>
<td>$R_{CB}$</td>
<td>0.25</td>
</tr>
<tr>
<td>$R_{DB}$</td>
<td>0.25</td>
</tr>
<tr>
<td>$R_{EB}$</td>
<td>0.75</td>
</tr>
<tr>
<td>$R_{FB}$</td>
<td>0.25</td>
</tr>
<tr>
<td>$R_{GB}$</td>
<td>0.75</td>
</tr>
<tr>
<td>$R_{HB}$</td>
<td>1.75</td>
</tr>
<tr>
<td>$R_{IB}$</td>
<td>0.75</td>
</tr>
</tbody>
</table>

Then, we plug them into formula 4.13 and get $\text{tau}=252.5\text{ps}$.
Let’s check with SPICE to see how accurate our answer is. We expect the 0%-90% rise time, to be $2.3*\text{tau} = 581\text{ps}$.
Here’s the spice deck describing our network.
Below is the plot of input and output. We see that the 0%-90% rise time is 580ps, which agrees almost perfectly with our prediction!
Problem #2

a. Compute the 0%-50% delay

i. Using a lumped model for the wire.
R = 100 ohms + 0.08 ohms/sq * L/W = 180 ohms.
C = 30aF*L*W + 40aF*2*L = 47.5 fF.
0.69 * RC = 5.9 ps.

ii. Using a PI model for the wire, and the Elmore equations to find tau.
PI model

\[
\text{Rw} \quad \text{Cw/2} \quad \text{Rw} \quad \text{Cw/2}
\]

\[
\text{Tau} = \text{Rs} \times \text{Cw/2} + (\text{Rs} + \text{Rw}) \times \text{Cw/2}
\]

0.69 * Tau = 4.59 ps.

iii. Using the distributed RC line equations from Chapter 4, section 4.4.4 (find 0%-50% point).

0.69 * Rs * Cw + 0.38 * Rw * Cw = 4.7 ps.

b) Compare your results in part a. using spice (be sure to include the source resistance). For each simulation, measure the 0%-50% time for the output
i) 6ps
ii) 5ps
iii) 4ps

See spice deck below:
Problem #3

a) What is the "critical length" of the wire.

Approximate the driver as a voltage source in series with a resistor.

\[ R_s \approx \frac{R_s + R_N}{2} = 5\, \text{Kohms} \]

The “critical length” is when the delay from the wire resistance is the same as the delay added by the wire capacitance alone. Using a PI model for the wire (shown below),...
...and using the Elmore delay equations, we get the delay at node X:

\[
\tau_X = \frac{C_w}{2} (R_s + \frac{C_w}{2} (R_s + R_w) = R_s C_w + \frac{R_w C_w}{2}
\]

We see that \(R_s C_w\) is the delay added by the wire capacitance alone, and \(\frac{R_w C_w}{2}\) is the extra delay added by the wire resistance. The critical delay is when they are equal, which is when \(L = \frac{2R_s}{r}\).

\[
r = \frac{80m\text{Ohms/sq}}{0.5\text{um}} = 0.16\text{Ohms/um}, \text{ so } L = 62.5\text{mm}.
\]

**b. What is the equivalent capacitance of a wire of this length?**

Total cap = area cap * L*W + fringe cap*2*L = **5.9pF**.
Problem #4

a. What is the propagation delay of the metal wire?

Rw = 10,000um/2.5um * 0.08 ohms/sq = 320 ohms.
Cw = 10000um*2.5um* 0.03fF/um² + 2*10000um*0.04fF/um = 1.55pf
Tau= 0.38*Rw*Cw = 188.5 ps

b. Compute the optimal size of the second inverter. What is the minimum delay through the buffer (i.e. the sum of the delays through both inverters)?

First, calculate $t_{po}$: 150 ps = $t_{po}(1+1/$gamma$)$ => $t_{po} = 75$ ps
Minimum delay $= t_{po}(1+u) + t_{po}(C_w/uC_i) = min => u = \sqrt{C_w/C_i} = 12.5$. Therefore, the second buffer should be 12.5 times the first one.
$T_{buf} = 2*(1+u)*t_{po} = 2.025$ ns.