Problem 1)

a) First, we need to find the skew between the source register clock ($\phi'$) and the destination register’s clock ($\phi''$). We can do this with a $\pi$2 model of the wire and the Elmore delay model.

\[
t_{\phi'} = 0.69 \times (150) \times (650 \, f) = 67 \, \text{ps}
\]
\[
t_{\phi''} = 0.69 \times [(150)(650 \, f) + (150+200)(950)] = 297 \, \text{ps}
\]
\[
\delta = t_{\phi''} - t_{\phi'} = 230 \, \text{ps} \quad (\text{eq. 9.1})
\]

Next, we check the race condition to see if the circuit will work properly. Note that the minimum logic delay is a single sum.

\[
\delta \leq t_{r,\text{min}} + t_i + t_{l,\text{min}} \quad (\text{eq. 9.2})
\]
\[
t_{\text{hold}} + \delta \leq t_{\text{clk-Q}} + t_{\text{sum}} \quad (\text{modified to include hold time and to use the given quantities})
\]
\[
100 + 230 \leq 300 + 50
\]
\[
330 \leq 350 \quad \text{TRUE (barely)... Thus, this circuit has no race problem}
\]

Lastly, we find the minimum clock period. Note that the maximum logic delay is a single sum plus the delay of the carry chain.

\[
T \geq t_{r,\text{max}} + t_i + t_{l,\text{max}} - \delta \quad (\text{eq. 9.3})
\]
\[
T \geq t_{\text{clk-Q}} + 31 \times t_{\text{carry}} + t_{\text{sum}} - \delta + t_{\text{setup}} \quad (\text{modified to include setup time and to use the given quantities})
\]
\[
T \geq 50 + (31)(250) + 300 - 230 + 150
\]
\[
T \geq 8.02 \, \text{ns}
\]
b) Identical to part a), except the capacitance at $\phi$" is much less.

\[ t_{\phi'} = 0.69 \times 150 \times 650 \text{ fF} = 67 \text{ ps} \]

\[ t_{\phi''} = 0.69 \times [ (150)(650 \text{ fF}) + (150+200)(350) ] = 152 \text{ ps} \]

\[ \delta = t_{\phi'} - t_{\phi} = 85 \text{ ps} \]

\[ t_{\text{hold}} + \delta \leq t_{\text{clk-Q}} + t_{\text{sum}} \]

\[ 100 + 85 \leq 300 + 50 \]

\[ 185 \leq 350 \quad \text{TRUE} \quad \text{... Thus, no race problem} \]

Note, however, that this circuit has a much better margin of error than the one from part (a).

\[ T \geq t_{\text{clk-Q}} + 31 \times t_{\text{carry}} + t_{\text{sum}} - \delta + t_{\text{setup}} \]

\[ T \geq 50 + (31)(250) + 300 - 85 + 150 \]

\[ T \geq 8.17 \text{ ns} \]

Note that the minimum cycle time is longer with the smaller skew.

c) Identical to (a), except that the clock is driven in the other direction.

\[ t_{\phi'} = 0.69 \times 150 \times 950 \text{ fF} = 98 \text{ ps} \]

\[ t_{\phi''} = 0.69 \times [ (150)(950 \text{ fF}) + (150+200)(650) ] = 255 \text{ ps} \]

\[ \delta = t_{\phi''} - t_{\phi} = -157 \text{ ps} \]

\[ t_{\text{hold}} + \delta \leq t_{\text{clk-Q}} + t_{\text{sum}} \]

\[ 100 - 157 \leq 300 + 50 \]

\[ -57 \leq 350 \quad \text{TRUE} \quad \text{... Thus, no race problem} \]

Note that this circuit has the best margin of error over all three cases.
\[ T \geq t_{\text{clk-q}} + 31t_{\text{carry}} + t_{\text{sum}} - \delta + t_{\text{setup}} \]
\[ T \geq 50 + (31)(250) + 300 + 157 + 150 \]
\[ T \geq 8.41 \text{ ns} \]

Note that the minimum cycle time is the longest over all three cases.

Problem 2)

a) To determine the max. period that we can clock this system, we need to examine every possible path between the synchronous latches and the associated delay.

<table>
<thead>
<tr>
<th>Source Latch</th>
<th>Destination Latch</th>
<th>Min Delay</th>
<th>Max Delay</th>
<th>Skew</th>
<th>Race Constraint</th>
<th>Clock Constraint</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 to L2</td>
<td>A, B</td>
<td>1ns+1.7ns=2.7ns</td>
<td>2.1ns+2.5ns=4.4ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L2 to L3</td>
<td>C, D</td>
<td>.5ns+2.2ns=2.7ns</td>
<td>1.4ns+2.9ns=4.3ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L2 to L4</td>
<td>C, E</td>
<td>.5ns+1.5ns=2.0ns</td>
<td>1.4ns+3.1ns=4.5ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L4 to L3</td>
<td>D</td>
<td>2.2ns</td>
<td>2.9ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L3 to L2</td>
<td>B</td>
<td>1.7ns</td>
<td>2.3ns</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

We want to focus on the minimum delay, because it is this factor which has the potential to through our system into a race condition.

We see that the shortest combinational path is 1.7ns from L3 \( \rightarrow \) L2. Since there is also a .3ns \( t_{\text{latch}} \). Thus our \( T_{\text{on}} \) must be within \( 1.7\text{ns} + .3\text{ns} = 2.0\text{ns} \)

b) For the Min. Period that we can clock the system we need to look at the max time:
\( T_{\text{min}} = \text{max(comb. Logic)} + t_{\text{latch}} = 4.5\text{ns} + .3\text{ns} = 4.8\text{ns} \)  (note: if there were a setup time specified, we would have to take that into account)

c) \( \text{Delay} = \sum \text{Block Delay} + t_{\text{latch}} \)

For min \( \delta \), use \( T_{\text{min}} = 4.5\text{ns} \) \( \Rightarrow \) consider L1 \( \rightarrow \) L2 case:
\( \delta > 0.2\text{ns} \)

For max \( \delta \), Consider L4 \( \rightarrow \) L3 case:
\( \delta < 4.5 - 3.2 \)
\( \delta < 1.3\text{ns} \)

For min \( \delta \), use \( T_{\text{min}} = 4.5\text{ns} \) \( \Rightarrow \) consider L1 \( \rightarrow \) L2 case:
\( \delta > 0.2\text{ns} \)

For max \( \delta \), Consider L4 \( \rightarrow \) L3 case:
\( \delta < 4.5 - 3.2 \)
\( \delta < 1.3\text{ns} \)

d) Note that with \( T = 5.0\text{ns} \), there is no longer a minimum skew requirement.

From the race constraint column, can see that limiting case is set by L2 \( \rightarrow \) L4 and L3 \( \rightarrow \) L2

\( T_{\text{on}} < 2.3 - 2\delta \)
\( T_{\text{on}} < \delta + 2.0 \)

Set \( 2.3 - 2\delta = 2.0 + \delta \Rightarrow \delta = 0.1 \)

\( T_{\text{on}} < 2.1 \)

Duty Cycle = \( 2.1/5.0 = 42\% \)
### Problem 3)

a) \[ L = 15\text{cm} \times 75 \cdot 10^{-10} \ \frac{H}{cm} = 112.5mH \]

\[
Z_0 = \sqrt{\frac{L}{C}}
\]

\[
C = \frac{L}{Z_0^2} = 11.25\text{pF}
\]

\[
\nu = \frac{1}{\sqrt{LC}} = \frac{88.9\text{cm}}{\text{us}}
\]

\[
\text{time of flight} = \frac{15\text{cm}}{\nu} = 169\text{ps}
\]

b) \[ R = \frac{35k}{200} = 175\Omega \]
\[ \rho = \frac{R_s - Z_0}{R_s + Z_0} = 0.27 \]

\[ V_{\text{in}} = 2.5 \times \frac{100}{275} = 0.91 \text{ V} + \text{initial voltage at the input of the line} \]

\[ V_{L1} = 0.91 + 0.27 \times 0.91 = 1.16 \text{ V} \]

\[ V_{L3} = 2.31 \text{ V} \]
After $t_r \rightarrow V_{L1} = 0.91 \times 2 = 1.82 \text{ V (perfect reflection)}$

After $3t_r \rightarrow V_{L3} = 1.82 + 0.27 \times 0.91 \times 2 = 2.31 \text{ V (within 10\%)}$

$\Rightarrow 3t_r = 507 \text{ ps}$

c) minimum delay is obtained for $R = Z_0 = 100\Omega$

$$\left(\frac{W}{L}\right)_a = \frac{35k}{100\Omega} = 350 = \left(\frac{87.5}{0.25}\right)$$

$$\left(\frac{W}{L}\right)_p = 1050 = \left(\frac{262.5}{0.25}\right)$$