Problem 1: Carry-skip adder

a) Design a 16-bit carry skip adder with equal group lengths using standard, complementary CMOS gates. Use a full adder cell as a building block for ripple-carry groups.

b) Assume that all gates (you have available: INV, NAND2, NOR2, XOR2, MUX2) have the same delays. Determine the optimal group length, k, as a function of adder length, n.

Problem 2: Timing & Race Conditions

The following circuit consists of a source portion which adds the outputs of two registers R1 & R2 and a destination portion which stores the sum in R3. The connections between the source and the destination are made by an automatic router which creates wires with an average length of 1 mm and containing an average of 10 contact holes in series. This leads to a resistance of about 200 Ω and capacitance of about 100 fF for each wire.

A clock driver buffers the clock signal at the source and is routed by the same tool to the destination, where it connects to R3 and two other registers (R4 & R5) which happen to be close by. Each register presents a load of 300 fF to the clock driver.

Assume the following timing values for the logic: \( t_{\text{carry}} = 250 \, \text{ps}, \, t_{\text{sum}} = 300 \, \text{ps} \) (including the wire load), \( t_{\text{setup}} = 150 \, \text{ps}, \, t_{\text{hold}} = 100 \, \text{ps}, \, t_{\text{clk-Q}} = 50 \, \text{ps} \).

a) Does this circuit have a race problem? What is the minimum clock period?

b) What if you removed R4 and R5? Would there be a race problem? What would the new minimum clock period be?

c) What if the driver were placed at the destination (with R3, R4 & R5)? Would there be a race problem? What would the new minimum clock period be?
Problem 3: Memory Cells

The 2-T memory cell uses 2 identical transistors with W/L = 0.3/0.2. Separate lines are provided for the read select (RS) and write select (WS), which both switch between 0 and 1.5V. The Bit Line is precharged to Vdd/2 prior to a read. A write is done by pulling the Bit Line either to Vdd or to GND. Ignore body effect and channel-length modulation. (γ=0; λ=0).

a) Explain the operation of the memory. Draw waveforms for BL, WS, and RS and Vx for reads and writes of both ‘1’s and ‘0’s.
b) Determine maximum current through transistors during a read operation.
c) The bit line is connected to a single-ended sense amp which would has a switching threshold of 200mV in either direction from Vdd/2. Compute the time required to read a data bit. Assume Cc=10fF and Cb=2pF.
Problem 4: DRAM Memory Cell

A single-transistor, DRAM cell is represented by the following circuit diagram. The bit line can be precharged to $V_{DD}/2$ by using a clocked precharge circuit. Also the WRITE circuit is assumed here to bring the potential of the bit line to $V_{DD}$ or 0V during the WRITE operation with word line at $V_{DD}$. Using the parameters given:

- $V_{To} = 1.0$ V
- $\gamma = 0.3 \ V^{1/2}$
- $|2\phi_F| = 0.6$V

a) Find the maximum voltage across the storage capacitor $C_s$ after WRITE-1 operation, i.e., when the bit line is driven to $V_{DD} = 5$V.

b) Assuming zero leakage current in the circuit, find the voltage at the bit line during READ-1 operation after the bit line is first precharged to $V_{DD}/2$. 

![Circuit Diagram](image-url)