Design Metrics

Last Lecture

- Moore’s law
- Challenges in digital IC design in the next decade.
Today: Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
  - design time and effort, mask generation
  - one-time cost factor
- Recurrent costs
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area
NRE Cost is Increasing

Die Cost

From http://www.amd.com
Cost per Transistor

Fabrication capital cost per transistor (Moore’s law)

Yield

\[ Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\% \]

Die cost = \[ \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}} \]

Dies per wafer = \[ \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{2 \times \text{die area}} \]
Defects

\[
\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}
\]

\(\alpha\) is approximately 3

\(\text{die cost} = f(\text{die area})^4\)

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Some Examples (1994)

<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Def./ Area</th>
<th>Dies/ wafer</th>
<th>Yield</th>
<th>Die cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>2</td>
<td>0.90</td>
<td>$900</td>
<td>1.0</td>
<td>81</td>
<td>54%</td>
<td>$4</td>
</tr>
<tr>
<td>486 DX2</td>
<td>3</td>
<td>0.80</td>
<td>$1200</td>
<td>2.0</td>
<td>81</td>
<td>54%</td>
<td>$12</td>
</tr>
<tr>
<td>Power PC 601</td>
<td>4</td>
<td>0.80</td>
<td>$1700</td>
<td>1.3</td>
<td>115</td>
<td>28%</td>
<td>$53</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>3</td>
<td>0.80</td>
<td>$1300</td>
<td>1.0</td>
<td>119</td>
<td>27%</td>
<td>$73</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>3</td>
<td>0.70</td>
<td>$1500</td>
<td>1.2</td>
<td>234</td>
<td>19%</td>
<td>$149</td>
</tr>
<tr>
<td>Super Sparc</td>
<td>3</td>
<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>13%</td>
<td>$272</td>
</tr>
<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>9%</td>
<td>$417</td>
</tr>
</tbody>
</table>
Administrivia

- Everyone should have a UNIX account on Cory! This will allow you to run HSPICE!
  - If not, check http://www-inst.eecs.berkeley.edu/usr/pub/jpg/How-to-Get-Named-Acct.jpg
- PC accounts for 353 Cory will be created early next week (when the classlist is completed)
- Discussions start in Week 2
- Labs start in Week 3!
- CHECK THE CLASS ROSTER ON THE WEB! Notify (ee141@bwrc.eecs.berkeley.edu) if errors.

Reliability
Noise in Digital Integrated Circuits

(a) Inductive coupling  (b) Capacitive coupling  (c) Power and ground noise
### DC Operation
**Voltage Transfer Characteristic**

![Graph showing DC Operation and Voltage Transfer Characteristic]

- $V_{OH}$
- $V_{OL}$
- $V_{OH} = f(V_{OL})$
- $V_{OL} = f(V_{OH})$
- $V_{M}$
- Switching Threshold
- Nominal Voltage Levels

### Mapping between analog and digital signals

![Graph showing mapping between analog and digital signals]

- "1": $V_{OH}$, $V_{IH}$
- Undefined Region
- "0": $V_{IL}$, $V_{OL}$
- Slope = -1
Definition of Noise Margins

Noise margin high

Noise margin low

Gate Output → Gate Input

Noise Budget

- Allocates gross noise margin to expected sources of noise
- Sources: supply noise, cross talk, interference, offset
- Differentiate between fixed and proportional noise sources
Key Reliability Properties

- Absolute noise margin values are deceptive
  » a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- Noise immunity is the more important metric – the capability to suppress noise sources
- Key metrics: Noise transfer functions, Output impedance of the driver and input impedance of the receiver;

Regenerative Property

Regenerative

Non-Regenerative
Regenerative Property

(a) A chain of inverters

(b) Simulated response of chain of MOS inverters

Fan-in and Fan-out

(a) Fan-out $N$

(b) Fan-in $M$
The Ideal Gate

\[ V_{\text{out}} = \begin{cases} \infty & \text{if } R_i = \infty \\ 0 & \text{if } R_o = 0 \\ \infty & \text{for Fanout} = \infty \\ \frac{V_{\text{DD}}}{2} & \text{if } \text{NM}_{\text{H}} = \text{NM}_{\text{L}} = \frac{V_{\text{DD}}}{2} \end{cases} \]

An Old-time Inverter

\[ V_{\text{out}}(V) \]
Delay Definitions

Ring Oscillator

\[ T = 2 \times t_p \times N \]
A First-Order RC Network

\[ v_{out}(t) = (1 - e^{-t/\tau}) V \]

\[ t_p = \ln(2) \quad \tau = 0.69 RC \]

Important model – matches delay of inverter

Power Dissipation

Instantaneous power:

\[ p(t) = v(t)i(t) = V_{supply}i(t) \]

Peak power:

\[ P_{peak} = V_{supply}i_{peak} \]

Average power:

\[ P_{ave} = \frac{1}{T} \int_t^{t+T} p(t)dt = \frac{V_{supply}}{T} \int_t^{t+T} i_{supply}(t)dt \]
Energy and Energy-Delay

Power-Delay Product (PDP) =

\[ E = \text{Energy per operation} = P_{av} \times t_p \]

Energy-Delay Product (EDP) =

quality metric of gate = \( E \times t_p \)

A First-Order RC Network

\[ E_{0\to1} = \int_{t=0}^{T} P(t) \, dt = V_{dd} \int_{0}^{T} i_{\text{supply}}(t) \, dt = V_{dd} \int_{0}^{T} C_L V_{out} \, dV_{out} = C_L \times V_{dd} \]

\[ E_{\text{cap}} = \int_{t=0}^{T} P_{\text{cap}}(t) \, dt = V_{dd} \int_{0}^{T} V_{out} \, dV_{out} = \int_{0}^{T} C_L V_{out} \, dV_{out} = \frac{1}{2} C_L \times V_{dd}^2 \]
Next Class (Prof. Vladimirescu)

- Introduction to the CMOS Inverter
- Devices models