Problem 1 – Extracting Unified Model Parameters from Simulation

The objective of this problem is to simulate a complex transistor model using SPICE, extract information from the results to build an approximate transistor model for use in hand calculations, and then compare the two models.

1A Using SPICE on the instructional computers, generate the family of I-V curves for an NMOS transistor with the following parameters:

W/L = 10\mu m/1\mu m
Sweep VDS from 0V to 2.0V in 0.1V increments
VGS = 0.4V, 0.8V, 1.2V, 1.6V, 2.0V
VSB = 0V, 1.0V

For this problem use a generic 0.5\mu m model by adding the following line to your SPICE deck or copying the same file to your own account or workstation:

```
.include `/home/aa/grad/bsl/MODELS/g50.mod`
```

1B Based on the results from the previous part, determine the following model parameters: \( V_{T0} \), \( k_p \), \( \lambda \), \( \gamma \). You may assume that velocity saturation doesn’t play a significant role and \(-2\Phi_F = 0.6V\).

1C Starting with the SPICE deck used in the first part, add your own simple transistor model using the parameters determined above. This should be of the form

```
.model nmos_simple NMOS (LEVEL = 1 + VT0=?? KP=?? GAMMA=?? LAMBDA=?? PHI=0.3)
```

Generate the family of I-V curves for an NMOS transistor with the following parameters, showing simulation of both the original model and your own simplified model on the same plot. Comment on any differences.

W/L = 1.0\mu m/0.25\mu m
Sweep VDS from 0V to 2.0V in 0.1V increments
VGS = 0.5V, 1.0V, 1.5V, 2.0V
VSB = 0.8V
Problem 2 – Generating a Voltage Transfer Characteristic

The circuit below features an NMOS transistor that is coupled to a non-linear load device represented by the shaded box. Accompanying the figure is the I-V characteristic for this non-linear load device, which is also given by the equation $I_{\text{box}} = \alpha V_{\text{box}}^{1/2}$, with the constant $\alpha = 0.3 \text{mA/}V^{1/2}$

The family of I-V curves for the NMOS transistor is given below:
2A  Draw the VTC for this circuit. Determine (or estimate, if necessary, from your VTC) the following parameters: $V_{OH}$, $V_{OL}$, $V_M$.

2B  This circuit can be used as an alternative to a traditional CMOS inverter (where the non-linear device is a PMOS transistor). From the concepts discussed thus far in lecture and from the results of your VTC, what are the disadvantages of this method?

Problem 3 – VTC and Noise Margins Analysis

A “Psuedo NMOS” inverter implementation is shown in Figure A, in which the load is a PMOS transistor with a fixed VGS. Figure B shows a standard CMOS inverter.

3A  Find $V_{OH}$, $V_{OL}$, and $V_M$ for the two inverters using the quadratic equations.

3B  Use HSPICE to plot the VTC of the two inverters. Compare the differences in the VTC curves, robustness, and regeneration (assuming the output will connect to another inverter of the same implementation) of the two inverters.

Use the following parameters:
- NMOS: $V_{TO} = 0.5V$, $k' = 18\mu A/V^2$, $\gamma = 0.5V^{1/2}$, $\lambda = 0.06V^{-1}$
- PMOS: $V_{TO} = 0.5V$, $k' = 5\mu A/V^2$, $\gamma = 0.5V^{1/2}$, $\lambda = 0.1V^{-1}$
Problem 4 – Energy

Consider the simple CMOS inverter model of Figure A, where switches 1 and 2 are assumed to have finite resistance $R$, and represent the PMOS and NMOS devices, respectively. The power supply is in the form of a battery.

**Figure A**

**Figure B**

4A How much energy is stored on the capacitor in Figure A when it is finished charging (a “long time” after switch 2 is opened and switch 1 is closed)?

4B Assuming the load capacitor started at zero initial charge, how much energy was supplied by the battery during this process?

4C Do the results for 4A and 4B agree? If not, explain why they are different and how efficient the charging process is (in terms of energy delivered to the capacitor vs. total energy supplied).

4D Now consider Figure B, where the capacitor is being charged to the same final voltage, but in two steps from two different batteries. First switch 2 is closed for a “long” time, then switch 2 is opened and switch 1 is closed. Repeat the calculations of parts A-C for this circuit.

4E Is $V_{DD}/2$ the optimal voltage for battery 2 in Figure B? If not, what is?

4F Now consider the need to discharge the load capacitor in Figure B back to ground. What is the optimal switch sequence? What is the net energy consumed from the two batteries for a complete cycle of charging and then discharging $C_L$? How does this compare to the net energy consumed for a complete cycle with the circuit in Figure A? Assume that the second battery is still $V_{DD}/2$ in this part.