Problem 1 – VTC of Inverter

a) Figure 1a depicts the $I_d - V_{OUT}$ curve of a typical NMOS transistor

Figure 1b depicts the $I_d - V_{OUT}$ curve of a typical PMOS transistor

Assume we use these FETs to create a CMOS inverter. Using this family of curves, graph the VTC, and calculate $V_{M}$, $V_{IL}$, and $V_{IH}$.

Top: Figure 1a, Bottom: Figure 1b

b) If we increase the W/L ratio of the pull-down NMOS (leaving the PMOS size fixed), in which direction will the VTC shift?
c) If instead, we increase the W/L ratio of the pull-up PMOS (and leave the NMOS the original size), in which direction will the VTC shift?

d) Please explain how the resizing in b) and c) will affect the above I-V curves in each case and give an intuitive explanation of how this affects the VTC of each.

**Problem 2 – Inverter Delay Calculation**

An old implementation of MOS inverters is shown in Fig. 2a, in which a diode-connected NMOS transistor is used as the load. The standard inverter implementation is shown in Fig. 2b. We are going to compare them on performance metric. Assume that both of them are driven by a standard inverter (the high input voltage is Vdd and low input voltage is 0). There is a capacitive load $C_L=150\text{fF}$ on the output node of each inverter, which is large compared to the parasitic capacitances of the devices.

a) For inverter A, prove that when the output voltage characteristics satisfy the following relation: $V_M \approx (V_{OH} + V_{OL})/2$, the delay for output to rise from $V_{OL}$ to $V_M$ (or fall from $V_{OH}$ to $V_M$) can be modeled as $t_p = 0.69R_{eq}C_L$, even if the output swing is not rail-to-rail. Here $R_{eq}$ is the equivalent resistance of the device driving the output, and $C_L$ is the load capacitance on the output node.

b) Evaluate the propagation delays of the two inverters by measuring the delay as the time between $V_{IN} = V_M$ and $V_{OUT} = V_M$. You will need to find $V_M$, $V_{OH}$ and $V_{OL}$ for each of these two inverters first. Use the switch approximation analysis of the MOS transistor presented in class ($R_{eq} = (R_M + R_{V_{OH}}) / 2$) to estimate $t_p\text{LH}$, and same for $t_p\text{HL}$.

c) Verify $t_p\text{LH}$ and $t_p\text{HL}$ using HSPICE. (Note that there may be slight difference between your SPCE and hand calculation results, because approximations are used in our hand analysis. You can think about the reason for the discrepancy while you are not required to do so in this homework.)

d) Explain why M2 is sized to be much smaller than M1 in the first (all-NMOS) circuit? Briefly comment on that. What disadvantages on performance does the inverter with NMOS-load have compared to the CMOS inverter?

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Use the following parameters:

NMOS: $V_{T0}=0.6\text{V}$, $k'=20\mu\text{A/V}^2$, $\gamma=0.5\text{V}^{1/2}$, $\lambda=0.05\text{V}^{-1}$;

PMOS: $V_{T0}=-0.6\text{V}$, $k'=7\mu\text{A/V}^2$, $\gamma=0.5\text{V}^{1/2}$, $\lambda=0.1\text{V}^{-1}$

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Left: Figure 2a: inverter A. Right: Figure 2b: Inverter B
Problem 3 – Computing the MOSFET Capacitances

a) It is always good to get a feel for design rules in a layout editor. Fire up Cadence Virtuoso with 0.24um technology. Place a minimum sized NMOS transistor and examine the dimensions. The layers are listed and shown below. Determine and list the following:
   a. Minimum Transistor Length
   b. Minimum Transistor Width
   c. Minimum Source/Drain Area
   d. Minimum Source/Drain Perimeter

   Please list the design rules you come across that lead to your results. (Refer to Lab2 for Cadence)

b) We desire a minimum sized CMOS inverter with a symmetrical VTC (V_M=V_D/2) with 0.24um technology. Calculate the following for the pull-up PMOS transistor in the design with the NMOS transistor minimum sized as in part a):
   a. Minimum Transistor Length
   b. Minimum Transistor Width
   c. Minimum Source/Drain Area
   d. Minimum Source/Drain Perimeter

   Assume the following:
   V_DD = 2.5V, V_M = 1.25V, and refer to Table 3.2 in the Book

c) Using the same minimum size inverter from part b), determine the input capacitance (i.e. the load it presents when driven). Please calculate the capacitance during a transition. From these, determine the total load capacitance that the inverter presents. Refer to Table 3.5 for capacitor parameters.
   *Hint: Consider the Miller effect

d) Using the g25 model provided in '/home/ff/ee141/MODELS/g25.mod', please verify the accuracy of your results in part c) by determining the total input capacitance in a high-low and a low-high transition with HSPICE and comparing with your total capacitance in part c). Turn in your HSPICE input deck.

   You'll notice there are four corners, TT, FF, SS, FS, and SF. These represent the different variation extremes we can expect due to process variations. For example, TT stands for NMOS: typical, PMOS: typical. FS stands for NMOS: fast, PMOS: slow etc. For this homework, please use the TT model.

   To use these models, include the following in your HSPICE deck:
   .lib '/home/ff/ee141/MODELS/g25.mod' TT

e) Determine V_{IH}, V_{IL}, N_{MH}, and N_{MI}.
   *Hint: The 2 parameters r and g vary proportionally with transistor width. The equations given are derived with the minimum width in mind. (Please refer to Eq’s 5.3 and 5.10 in the book for r and g)