Problem 1 – Extracting Unified Model Parameters from Simulation

The objective of this problem is to simulate a complex transistor model using SPICE, extract fundamental information from the results to build an approximate transistor model for use in hand calculations, and then compare the two models.

1A Using SPICE, generate the family of I-V curves for an NMOS transistor with the following parameters:

- W/L = 10μm/1μm
- Sweep VDS from 0V to 2.0V in 0.1V increments
- VGS = 0.4V, 0.8V, 1.2V, 1.6V, 2.0V
- VSB = 0V, 1.0V

For this problem use a generic 0.5um model by adding the following line to your SPICE deck or copying the same file to your own account or workstation:

```
.include '/home/aa/grad/bsl/MODELS/g50.mod'
```

Soln: The following Spice deck is written to generate the family of curves:

```
* EE141 SPRING 2004 HW2 PROB 1A
* Generates family of I-V curves for a given NMOS model
* Reference transistor model
.include '/home/aa/grad/bsl/MODELS/g50.mod'

* paramters
.param sb = 0

* Netlist to probe the transistor
M1 drain gate source bulk NMOS w=10u l=1u

* three DC voltage sources to apply test signals
VDS drain 0 0
VGS gate source 0
VSB source bulk sb

* connect the source to ground with a 0 V source
VSOURCE source 0 0

* format output for use in AWaves
.options post=2
```
* DC sweep with VDS as the inner sweep, and outer loops set different values for VGS and VSB. Recall that the source terminal is fixed at 0 potential.

```
.DC VDS 0 2 0.1 VGS 0.4 2 0.4
.alter
.param sb = 0
.alter
.param sb = 1
.end
```

The Spice deck is simulated with HSpice, and the resulting plot is generated in AWaves:

**1B** Based on the results from the previous part, determine the following model parameters: $V_{T0}$, $k_p$, $\lambda$, $\gamma$. You may assume that velocity saturation doesn’t play a significant role and $-2\Phi_F = 0.6V$.

**Soln:** There are multiple ways to extract these parameters, but a simple method is as follows.

$V_{T0}$: Select two points in the saturation region from different VGS curves, but with VSB=0 and the same VDS in both cases. This allows us to extract $V_{T0}$ from
the unified model equations. The points can be measured directly in AWaves or graphically from the result in 1A.

<table>
<thead>
<tr>
<th>Point</th>
<th>( V_{GS} )</th>
<th>( V_{DS} )</th>
<th>( I_D )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.2V</td>
<td>1.5V</td>
<td>197uA</td>
</tr>
<tr>
<td>B</td>
<td>1.6V</td>
<td>1.5V</td>
<td>517uA</td>
</tr>
</tbody>
</table>

\[
\frac{I_{DA}}{I_{DB}} = \frac{1}{2} k p \frac{W}{L} (V_{GSA} - V_{T0})^2 (1 + \lambda V_{DSA}) = \frac{(V_{GSA} - V_{T0})^2}{(V_{GSA} - V_{T0})^2} = \left(1 + \lambda V_{DSA}\right)
\]

\[
\frac{197}{517} = \frac{(1.2 - V_{T0})^2}{(1.6 - V_{T0})^2}
\]

\( V_{T0} = 0.555V \)

\( \lambda \) is extracted with the same method, this time picking two points with the same VGS but differing VDS:

<table>
<thead>
<tr>
<th>Point</th>
<th>( V_{GS} )</th>
<th>( V_{DS} )</th>
<th>( I_D )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.6V</td>
<td>1.4V</td>
<td>516uA</td>
</tr>
<tr>
<td>B</td>
<td>1.6V</td>
<td>2.0V</td>
<td>521uA</td>
</tr>
</tbody>
</table>

\[
\frac{I_{DA}}{I_{DB}} = \frac{1}{2} k p \frac{W}{L} (V_{GSA} - V_{T0})^2 (1 + \lambda V_{DSA}) = \frac{(1 + \lambda V_{DSA})}{(1 + \lambda V_{DSA})} = \frac{516}{521} = \frac{(1 + 1.4\lambda)}{(1 + 2\lambda)}
\]

\( \lambda = 0.0165V^{-1} \)

\( \gamma \) is extracted the same way again, but this time keep VGS and VDS constant and vary VSB:

<table>
<thead>
<tr>
<th>Point</th>
<th>( V_{SB} )</th>
<th>( V_{GS} )</th>
<th>( V_{DS} )</th>
<th>( I_D )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0V</td>
<td>1.6V</td>
<td>2.0V</td>
<td>521uA</td>
</tr>
<tr>
<td>B</td>
<td>1V</td>
<td>1.6V</td>
<td>2.0V</td>
<td>279uA</td>
</tr>
</tbody>
</table>
\[
\frac{I_{D1}}{I_{D2}} = \frac{1}{2} k_p \frac{W}{L} \left( V_{GSA} - V_{T0} \right)^2 \left( 1 + \lambda V_{DSA} \right)
\]

\[
\frac{I_{D2}}{I_{D3}} = \frac{1}{2} k_p \frac{W}{L} \left( V_{GSB} - V_T \right)^2 \left( 1 + \lambda V_{DSB} \right)
\]

\[
\frac{521}{279} = \frac{(1.6 - 0.555)^2}{(1.6 - V_T)^2}
\]

\[
V_T = 0.835V
\]

Now, use the body effect formula:

\[
V_T - V_{T0} = \gamma \left( \sqrt{V_{SB} - 2 \Phi_F} - \sqrt{-2 \Phi_F} \right)
\]

\[
0.835 - 0.55 = \gamma \left( \sqrt{1.6} - \sqrt{0.6} \right)
\]

\[
\gamma = 0.571V^{1/2}
\]

\[
k_p \text{ is found by plugging a single point into the saturation current equation:}
\]

<table>
<thead>
<tr>
<th>Point</th>
<th>VSB</th>
<th>VGS</th>
<th>VDS</th>
<th>ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0V</td>
<td>1.6V</td>
<td>2.0V</td>
<td>521uA</td>
</tr>
</tbody>
</table>

\[
I_{D1} = \frac{1}{2} k_p \frac{W}{L} \left( V_{GSA} - V_{T0} \right)^2 \left( 1 + \lambda V_{DSA} \right)
\]

\[
521uA = \frac{1}{2} k_p \cdot 10 \cdot (1.6V - 0.555V)^2 (1 + 0.0165V^{-1} \cdot 2V)
\]

\[
k_p = 92.4uA/V^2
\]

1C Starting with the SPICE deck used in the first part, add your own simple transistor model using the parameters determined above. This should be of the form

```
.model nmos_simple NMOS (LEVEL = 1
+ VT0=?? KF=?? GAMMA=?? LAMBDA=?? PHI=0.3)
```

Typo: should have been PHI=0.6. Should only have a minor impact on the solutions though.

Generate the family of I-V curves for an NMOS transistor with the following parameters, showing simulation of both the original model and your own simplified model on the same plot. Comment on any differences.
Sweep VDS from 0V to 2.0V in 0.1V increments
VGS = 0.5V, 1.0V, 1.5V, 2.0V
VSB = 0.8V

Soln: The new spice deck is as follows:

* EE141 SPRING 2004 HW2 PROB 1C
* Generates family of I-V curves for a given NMOS model
  * and a simpler approximate model

* Reference transistor model
.include '/home/aa/grad/bsl/MODELS/g50.mod'

* approximate model
.model nmos_simple NMOS (LEVEL = 1
+ VT0=0.555 KP=92.4e-6 GAMMA=0.571 LAMBDA=0.0165 PHI=0.3)

* parameters
.param sb = 0

* Netlist to probe the two transistors
M1 drain gate source bulk NMOS w=10u l=1u
M2 drain gate source2 bulk nmos_simple w=10u l=1u

* three DC voltage sources to apply test signals
VDS drain 0 0
VGS gate source 0
VSB source bulk sb

* connect the sources to ground with 0 V supplies
* this fixes the absolute voltage levels in the circuit wrt ground
* and also provides a way to measure the drain current, because
* hspice will save the currents through these supplies
VSOURCE source 0 0
VSOURCE2 source2 0 0

* format output for use in AWaves
.options post=2

* DC sweep with VDS as the inner sweep, and outer loops
  * set different values for VGS and VSB. Recall
  * that the source terminal is fixed at 0 potential.
.DC VDS 0 2 0.1 VGS 0.4 2 0.4
.end

AWaves is used to plot the resulting two families on a single plot shown below. There are two main differences:
1) In the saturation region the level 1 model predicts too much current for high VGS, too little current for low VGS
2) In most cases the current in the linear region is too low in the simple model, even for gate voltages where the saturation current is close to the original model. Another way of looking at this is that in the linear region the level 1 model
generally predicts a weaker device, but the linear region extends to higher values of VDS.

These differences are consistent with the fact that short channel effects are neglected in the level 1 model, but not the original model. Compared with the quadratic level 1 model, we see that Ids grows slower than quadratic with VGS-VT in the full model, and saturation is reached at lower values of VDS for a given VGS.

The slope of the curves in the saturation region is similar in both models.

Note: Students who used W/L = 1.0u/0.25u as in the original handout may have very different qualitative solutions with more short channel effects visible.
Problem 2 – Generating a Voltage Transfer Characteristic

The circuit below features an NMOS transistor that is coupled to a non-linear load device represented by the shaded box. Accompanying the figure is the I-V characteristic for this non-linear load device, which is also given by the equation $I_{\text{box}} = \alpha V_{\text{box}}^{1/2}$, with the constant $\alpha = 0.3 \text{mA} / \sqrt{\text{V}}$

The family of I-V curves for the NMOS transistor is given below:
2A Draw the VTC for this circuit. Determine (or estimate, if necessary, from your VTC) the following parameters: \( V_{OH}, V_{OL}, V_M. \)

Soln: This is done by recognizing that \( V_{box} = 2.5V - V_{DS} \) and that \( I_{box} = I_D \), so the I-V curve for the box can be plotted as a load line against the NMOS family of curves as follows (this can be done by hand):

Noting that \( I_{box} = I_{drain} \) always, the operating points are the intersections of these two curves. These intersection points can be estimated by inspection:

<table>
<thead>
<tr>
<th>( V_{in} (VGS) )</th>
<th>( V_{out} (VDS) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>2.5V</td>
</tr>
<tr>
<td>0.4V</td>
<td>2.5V</td>
</tr>
<tr>
<td>0.7V</td>
<td>2.45V</td>
</tr>
<tr>
<td>1.0V</td>
<td>2.25V</td>
</tr>
<tr>
<td>1.3V</td>
<td>1.75V</td>
</tr>
<tr>
<td>1.6V</td>
<td>0.7V</td>
</tr>
<tr>
<td>1.9V</td>
<td>0.45V</td>
</tr>
<tr>
<td>2.2V</td>
<td>0.35V</td>
</tr>
<tr>
<td>2.5V</td>
<td>0.3V</td>
</tr>
</tbody>
</table>

These points form the VTC, which is plotted below (can be hand drawn also – it’s just an estimate anyway).
From the intersection points listed in the table we can see that $V_{OH} \approx 2.5\text{V}$, $V_{OL} \approx 0.3\text{V}$. From the VTC we can estimate that $V_M \approx 1.4\text{V}$, reasonably close to mid supply.

2B This circuit can be used as an alternative to a traditional CMOS inverter (where the non-linear device is a PMOS transistor). From the concepts discussed thus far in lecture and from the results of your VTC, what are the disadvantages of this method?

Soln: There are several disadvantages.
- There is static power consumed when Vin is high (over 1mW)
- $V_{OL} \neq 0$, so noise margins are reduced from optimal. (Although they are still roughly symmetric: $V_M$ and $V_{OL}$ are both skewed in the same direction).
- Regeneration isn’t very strong – the peak gain in the transition region is approximately $(1.75-1.05)/(1.6-1.3) = 3.5$. This also leads to lower noise margins than a standard inverter.
Problem 3 – VTC and Inverter Analysis

A “Psuedo NMOS” inverter implementation is shown in Figure A, in which the load is a PMOS transistor with a fixed VGS. Figure B shows a standard CMOS inverter.

3A Find $V_{OH}$, $V_{OL}$, and $V_M$ for the two inverters using the quadratic equations.

3B Use HSPICE to plot the VTC of the two inverters. Compare the differences in the VTC curves, robustness, and regeneration (assuming the output will connect to another inverter of the same implementation) of the two inverters.

![Figure A](image1.png)  
![Figure B](image2.png)

Use the following parameters:

**NMOS:** $V_{T0}=0.5V$, $k_p=18uA/V^2$, $\gamma=0.5V^{1/2}$, $\lambda=0.06V^{-1}$

**PMOS:** $V_{T0}=0.5V$, $k_p=5uA/V^2$, $\gamma=0.5V^{1/2}$, $\lambda=0.1V^{-1}$

**Soln:** 3A: Consider Figure A. First assume that $V_{OL}<0.5V$ because we know that the NMOS device is much stronger than the PMOS device for a full VDD input (MUST remember to verify this assumption after finding the solution). In this case we immediately note that $V_{OH}=V_{DD}=2.5V$, because when $V_{IN}=V_{OL}$ the NMOS device is in the cutoff region ($I_D=0$) and the PMOS device provides a conductive path to $V_{DD}$. Now, we find $V_{OL}$ by solving for $V_{out}$ when $V_{in}=V_{OH}=2.5V$. Again, with the assumption that $V_{OL}<0.5V$, note that the PMOS device will be in saturation because $|V_{DS}|>|V_{GS}-V_{TH}|$ and $|V_{GS}|>|V_{TH}|$. Thus, the PMOS drain current is given by:

$$I_{DP} = \frac{1}{2} k_p \left( \frac{W}{L} \right) (V_{GS} - V_{T0P})^2 (1 + \lambda_p V_{DSP})$$
\[ I_{D_P} = 20\mu A \cdot (1 + 0.1V^{-1}(V_{DD} - V_{OL})) \]

\[ I_{D_P} = \frac{25\mu A}{V} \cdot V \cdot V_{OL} \]

Following the same assumption, the NMOS device is in the triode (linear) region because \(V_{DS} < V_{GS} - V_{TH}\) and \(V_{GS} > V_{TH}\). Thus, the drain current for the NMOS device is given by:

\[ I_{D_N} = k p_n \left( \frac{W}{L} \right)_n \left( (V_{GS} - V_{TH}) \cdot V_{OL} - \frac{V_{OL}^2}{2} \right) \]

\[ I_{D_N} = \frac{54\mu A}{V^2} \left( 2V \cdot V_{OL} - \frac{V_{OL}^2}{2} \right) \]

\[ I_{D_N} = \frac{108\mu A}{V} \cdot V_{OL} - \frac{27\mu A}{V^2} \cdot V_{OL}^2 \]

Equating the NMOS and PMOS drain currents we have

\[ 25\mu A - \frac{2\mu A}{V} \cdot V_{OL} = \frac{108\mu A}{V} \cdot V_{OL} - \frac{27\mu A}{V^2} \cdot V_{OL}^2 \]

\[ \frac{27\mu A}{V^2} \cdot V_{OL}^2 - 110\mu A \cdot V \cdot V_{OL} + 25\mu A = 0\mu A \]

Using the quadratic formula to solve for \(V_{OL}\) we find two roots: 3.83V and 242mV. The first root is mathematically inconsistent with our assumptions – if that was the answer, the equations used to model the NMOS and PMOS currents wouldn’t be correct any more. However, the other root is consistent with the equations used to this point. Therefore,

\( V_{OL} = 242\text{mV for Figure A} \)

Note that this solution for \(V_{OL}\) is consistent with the original assumption (< 0.5V), validating the previous solution for \(V_{OH}\). I.e., the two values found for \(V_{OH}\) and \(V_{OL}\) can be shown to simultaneously satisfy both relationships \(V_{OL} = f(V_{OH})\) and \(V_{OH} = f(V_{OL})\).

To find \(V_M\), we follow a similar pattern of assumption followed by verification. Assume that \(V_M > 0.5V\), in which case the PMOS device will be operating in the triode region. Since \(Vin = Vout = V_M\) at the midpoint, we see that \(V_{GS} = V_{DS}\) for the NMOS device, so it is now operating in the saturation region. The PMOS drain current is now given by:
The NMOS drain current is now given by:

\[ I_{DP} = k_p \left( \frac{W}{L} \right) \left( |V_{GSP}| - |V_{T0P}| \right) \cdot \left( V_{DD} - V_M \right) - \frac{(V_{DD} - V_M)^2}{2} \]

\[ I_{DP} = 10 \mu A/V^2 \left( 2V \cdot (V_{DD} - V_M) - \frac{(V_{DD} - V_M)^2}{2} \right) \]

\[ I_{DP} = 20 \mu A/V \cdot (V_{DD} - V_M) - 5 \mu A/V^2 \cdot (V_{DD} - V_M)^2 \]

\[ I_{DP} = 50 \mu A - 20 \mu A/V \cdot V_M - 5 \mu A/V^2 \cdot \left( V_{DD}^2 - 2V_{DD}V_M + V_M^2 \right) \]

\[ I_{DP} = 18.75 \mu A + 5 \mu A/V \cdot V_M - 5 \mu A/V^2 \cdot V_M^2 \]

The NMOS drain current is now given by:

\[ I_{DN} = \frac{1}{2} k_p \left( \frac{W}{L} \right) \left( V_M - V_{T0N} \right)^2 (1 + \lambda_N V_M) \]

\[ I_{DN} = 27 \mu A/V^2 (V_M - 0.5V)^2 (1 + 0.06V^{-1} \cdot V_M) \]

\[ I_{DN} = 27 \mu A/V^2 (V_M^2 - 1V \cdot V_M + 0.25V^2) (1 + 0.06V^{-1} \cdot V_M) \]

\[ I_{DN} = 1.62 \mu A/V^3 \cdot V_M^3 + 25.38 \mu A/V^2 \cdot V_M^2 - 26.59 \mu A/V \cdot V_M + 6.75 \mu A \]

We follow a similar procedure of equating the drain currents for the two devices, but now we are left with a cubic equation:

\[ 1.62 \mu A/V^3 \cdot V_M^3 + 30.38 \mu A/V^2 \cdot V_M^2 - 31.59 \mu A/V \cdot V_M - 12 \mu A = 0 \mu A \]

Solving numerically with Mathematica, MATLAB, MathCad, etc., the roots of this equation are found to be -19.7V, -0.30V, and 1.27V. Only the last solution is consistent with the operating modes that our equations represent, so this is the solution. Note that it is also consistent with the previous assumption that \( V_M > 0.5V \). Therefore,

\[ V_M = 1.27V \text{ for Figure A} \]

In the case of the CMOS inverter, it was shown in class that \( V_{OH} = V_{DD} = 2.5V \) and \( V_{OL} = 0V \). For the midpoint voltage, note that both the NMOS and the PMOS devices must be in saturation, as they both have \( V_{GS} = V_{DS} \) and it is not possible
for one device to be cutoff. Thus, the NMOS drain current equation is the same as it was in the previous circuit:

\[ I_{DN} = 1.62uA/V^3 \cdot V_M^3 + 25.38uA/V^2 \cdot V_M^2 - 26.59uA/V \cdot V_M + 6.75uA \]

The PMOS drain current is given by:

\[ I_{DP} = \frac{1}{2} k_P \left( \frac{W}{L} \right)_P \left( V_{GSP} - V_{T0P} \right)^2 \left( 1 + \lambda_P V_{DSP} \right) \]

\[ I_{DP} = 15uA/V^2 \left( (2.5V - V_M) - 0.5V \right)^2 \left( 1 + 0.1V^{-1} (V_{DD} - V_M) \right) \]

\[ I_{DP} = 15uA/V^2 \left( 4V^2 - 4V_M + V_M^2 \right) \left( 1.25 - 0.1V^{-1} V_M \right) \]

\[ I_{DP} = 1.5uA/V^3 \cdot V_M^3 + 12.75uA/V^2 \cdot V_M^2 - 69uA/V \cdot V_M + 75uA \]

Equating these two drain currents we have:

\[ 0.12uA/V^3 \cdot V_M^3 + 12.63uA/V^2 \cdot V_M^2 + 42.41uA/V \cdot V_M - 68.25uA = 0uA \]

Again, solving this cubic equation numerically, the logical solution is found to be:

\[ V_M = 1.19V \] for Figure B.

3B The following Spice netlist is created to simulate the VTCs for these two inverters:

```verbatim
* EE141   SPRING 2004   HW2   PROB 3
.model nmos NMOS (LEVEL = 1
+ VTO = 0.5  KP = 18e-6  GAMMA = 0.5  LAMBDA = 0.06  PHI = 0.3)
.model pmos PMOS (LEVEL = 1
+ VTO = -0.5  KP = 5e-6  GAMMA = 0.5  LAMBDA = 0.1  PHI = 0.3)
*Psuedo NMOS netlist
M1 vout_pn 0 vdd vdd pmos W=1u L=0.5u
M2 vout_pn vin 0 0 nmos W=1.5u L=0.5u
*Standard Inverter netlist
M3 vout_std vin vdd vdd pmos w=3u l=0.5u
M4 vout_std vin 0 0 nmos w=1u l=0.5u
*Sources
VSUPP vdd 0 2.5
VSRRC vin 0 0
.options post=2
.op
```
AWaves is used to plot the simulation results:

From this plot we see that \( V_{OL} \) is close to the calculated value for the Psuedo-NMOS inverter, and that the standard inverter has a slightly lower transition voltage than the Psuedo-NMOS inverter, also in agreement with the above calculations.

Comparing these two VTC curves, we see that the standard inverter has

- Stronger regeneration (higher gain in the transition region)
- Lower \( V_{OL} \)

both of which lead to higher noise margins and better robustness.
**Problem 4 – Energy**

Consider the simple CMOS inverter model of Figure A, where switches 1 and 2 are assumed to have finite resistance R, and represent the PMOS and NMOS devices, respectively.

**Figure A**

**Figure B**

4A How much energy is stored on the capacitor in Figure A when it is finished charging (a long time after switch 2 is opened and switch 1 is closed)?

Soln: From basic physics and as seen in class, \( E_{\text{stored}} = \frac{1}{2} C_L V_{DD}^2 \)

4B Assuming the load capacitor started at zero initial charge, how much energy was supplied by the power supply during this process?

Soln: \( E_{\text{supplied}} = Q_{\text{supplied}} V_{DD} = Q_{\text{capacitor}} V_{DD} = (C_L V_{DD}) V_{DD} = C_L V_{DD}^2 \)

4C Do the results for 4A and 4B agree? If not, explain why they are different and how efficient the charging process is (in terms of energy delivered to the capacitor vs. total energy supplied).

Soln: They do not agree. The difference is energy that is lost in the switch resistance during charging (as heat). The energy efficiency is:

\[
\eta = \frac{E_{\text{stored}}}{E_{\text{supplied}}} = 0.5, \text{ or } 50\%
\]

4D Now consider Figure B, where the capacitor is being charged to the same final voltage, but in two steps. First switch 2 is closed for a “long” time, then switch 2 is opened and switch 1 is closed. Repeat calculations A-C for this case.

Soln:  
A) \( E_{\text{stored}} = \frac{1}{2} C_L V_{DD}^2 \)  
B) \( E_{\text{supplied}} = Q_{\text{supplied, BATT2}} V_{DD}/2 + Q_{\text{supplied, BATT1'}} V_{DD} = (C_L V_{DD}/2) V_{DD}/2 + (C_L (V_{DD} - V_{DD}/2)) V_{DD} = \frac{3}{4} C_L V_{DD}^2 \)

C) \( \eta = \frac{E_{\text{stored}}}{E_{\text{supplied}}} = 2/3, \text{ or } \sim 67\% \).
4E Is VDD/2 the optimal voltage for second supply in Figure B? If not, what is?

Soln: To find the optimal voltage, represent the voltage on battery 2 by $V_X$. Now minimize $E_{\text{supplied}} = C_L V_X^2 + C_L (V_{\text{DD}} - V_X) V_{\text{DD}}$ with respect to $V_X$:

$$\frac{dE_{\text{supplied}}}{dV_X} = 2C_L V_X - C_L V_{\text{DD}} = 0 \Rightarrow V_X = V_{\text{DD}}/2$$ is a local extrema.

Since there is only one local extrema, it must also be a global extrema, and since we know of another value of $V_X$ that leads to higher energy consumption, this extrema must be a minima. Therefore, the value of $V_{\text{DD}}/2$ is the global optimum.

4F Now consider the need to discharge the load capacitor in Figure B back to ground. What is the optimal switch sequence? What is the net energy consumed from the two supplies for a complete cycle of charging and then discharging $C_L$? How does this compare to the net energy consumed for a complete cycle with the circuit in Figure A? Assume that the second supply is still at $V_{\text{DD}}/2$ in this part.

Soln: The trick here is to recognize that the batteries can store as well as provide energy, and we can recover some of the energy stored in the capacitor back into battery 2 when discharging the capacitor. The optimal switch sequence is to
1) open switch 1 & close switch 2
2) open switch 2 & close close switch 3.

The energy recovered during step 1 is given by
$$E_{\text{recovered}} = Q_{\text{recovered}} V_{\text{DD}}/2 = (C_L (V_{\text{DD}} - V_{\text{DD}}/2)) V_{\text{DD}}/2 = \frac{1}{4} C_L V_{\text{DD}}^2$$

The net energy supplied is given by
$$E_{\text{net}} = E_{\text{supplied}} - E_{\text{recovered}} = \frac{1}{2} C_L V_{\text{DD}}^2$$

This is one half of the energy supplied using the circuit in Figure A.