EE141-Spring 2004
Digital Integrated Circuits

Lecture 17
PTL
Dynamic Logic

Administrative Stuff

- No Lab this week
- Hw 6 posted – Due April 1
- Project due Fr by 5:30pm
  - Electronic reports only!
  - Send report (using template from web-site) to ee141@cory.eecs.berkeley.edu
  - Do NOT forget to include your SPICE file
- Will be out of town on Th. Lecture by Prof. Vladimirescu on adders
Schedule

- Last lecture: project intro, PTL
- Today:
  - Dynamic Logic

Pass-Transistor Logic
Pass-Transistor Logic

- N transistors
- No static consumption

NMOS Only Logic: Level Restoring Transistor

- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem
**Restorer Sizing**

- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack

**Solution 2: Single Transistor Pass Gate with $V_T=0$**

*Watch out for leakage currents*
Complementary Pass Transistor Logic

Solution 3: Transmission Gate
**Resistance of Transmission Gate**

![Graph showing the resistance of transmission gate](image)

**Delay in Transmission Gate Networks**

![Schematic diagrams showing delay in transmission gate networks](image)
Delay Optimization

- Delay of RC chain
  \[ t_p = 0.69 \sum_{k=0}^{n} \frac{C_{eq}}{R_{eq}} k = 0.69 C_{eq} \frac{n(n+1)}{2} \]

- Delay of Buffered Chain
  \[ t_p = 0.69 \left[ \frac{n}{m} C_{eq} \frac{m(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right) t_{buf} \]
  \[ m_{opt} = 1.7 \frac{t_{buf}}{C_{eq}} \]

Transmission Gate Full Adder

Similar delays for sum and carry
Dynamic Logic

Dynamic CMOS

- In **static** circuits at every point in time (except when switching) the output is connected to either GND or $V_{DD}$ via a low resistance path.
  - fan-in of $n$ requires $2n \times (n \text{ N-type} + n \text{ P-type})$ devices

- **Dynamic** circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires on $n + 2 \times (n+1 \text{ N-type} + 1 \text{ P-type})$ transistors
Dynamic Gate

Two phase operation
Precharge (CLK = 0)
Evaluate (CLK = 1)

Dynamic Gate

Two phase operation
Precharge (Clk = 0)
Evaluate (Clk = 1)
**Conditions on Output**

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on $C_L$.

**Properties of Dynamic Gates**

- Logic function is implemented by the PDN only
  - number of transistors is $N + 2$ (versus $2N$ for static complementary CMOS)
- Full swing outputs ($V_{OL} = GND$ and $V_{OH} = V_{DD}$)
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds
  - reduced load capacitance due to lower input capacitance ($C_{in}$)
  - reduced load capacitance due to smaller output loading ($C_{out}$)
  - no $I_{sc}$, so all the current provided by PDN goes into discharging $C_L$
Properties of Dynamic Gates

- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between $V_{DD}$ and GND (including $P_{sc}$)
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- PDN starts to work as soon as the input signals exceed $V_{tn}$, so $V_{M}$, $V_{IH}$ and $V_{IL}$ equal to $V_{tn}$
  - low noise margin ($NM_L$)
- Needs a precharge/evaluate clock

Issues in Dynamic Design 1: Charge Leakage

Dominant component is subthreshold current
Solution to Charge Leakage

![Diagram of a circuit with labels: Clk, M, A, B, C_L, Out, Keeper.]

Same approach as level restorer for pass-transistor logic

Issues in Dynamic Design 2: Charge Sharing

![Diagram of a circuit with labels: Clk, M, A, B, C_L, C_A, C_B, Out.]

Charge stored originally on $C_L$ is redistributed (shared) over $C_L$ and $C_A$ leading to reduced robustness
**Charge Sharing Example**

Clk → Out

- \( C_a = 15\text{fF} \)
- \( C_b = 15\text{fF} \)
- \( C_c = 15\text{fF} \)
- \( C_d = 10\text{fF} \)
- \( C_L = 50\text{fF} \)

\[ \text{Clk} \quad \text{Out} \quad \text{Clk} \]

**Charge Sharing**

**Case 1** if \( \Delta V_{out} < V_{Tn} \)

\[
C_L V_{DD} = C_L V_{out}(t) + C_a (V_{DD} - V_{Tn}(V_X))
\]

or

\[
\Delta V_{out} = V_{out}(t) - V_{DD} = \frac{C_a}{C_L} (V_{DD} - V_{Tn}(V_X))
\]

**Case 2** if \( \Delta V_{out} > V_{Tn} \)

\[
\Delta V_{out} = -V_{DD} \left( \frac{C_a}{C_a + C_L} \right)
\]
**Solution to Charge Redistribution**

Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)

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**Issues in Dynamic Design 3: Backgate Coupling**

Dynamic NAND

Static NAND
**Backgate Coupling Effect**

![Backgate Coupling Effect](image)

**Issues in Dynamic Design 4: Clock Feedthrough**

Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above $V_{DD}$. The fast rising (and falling edges) of the clock couple to Out.
**Clock Feedthrough**

![Clock Feedthrough Diagram]

**Other Effects**

- Capacitive coupling
- Substrate coupling
- Minority charge injection
- Supply noise (ground bounce)
Next Lecture

- Arithmetic circuits and adders