EE141- Spring 2004
Digital Integrated Circuits

Lecture 20
Power
Sequential Logic - Intro

Administrative Stuff

- Midterm 2 Th 6:30pm in 277 Cory
  Material:
  - Wires
  - Complex logic
  - Arithmetic
- Review session on We at 5:30pm in 241 Cory
- Homework 7 posted – Due April 15
Class Material

- Last lecture
  - Multipliers – Shifters – Power Intro
- Today’s lecture
  - Power
  - Intro to sequential logic

Power
Power Dissipation in CMOS

- Dynamic power
  - Charging capacitances
  - Dominant today
- Leakage power
  - Leaky transistors
  - Concern in low-activity, portable devices
- Short circuit power
- Static power
  - E.g. pseudo-NMOS

Dynamic Power Consumption

\[
E_{0 \rightarrow 1} = \int_0^T P_{DD}(t)dt = V_{DD} \int_0^T i_{DD}(t)dt = V_{DD} \int_0^T C_L dV_{out} = C_L V_{DD}^2
\]

\[
E_C = \int_0^T P_C(t)dt = \int_0^T V_{out}i_L(t)dt = \int_0^T C_L V_{out} dV_{out} = \frac{1}{2} C_L V_{DD}^2
\]
**Dynamic Power Consumption**

Power = Energy/transition • Transition rate

\[
= C_L V_{DD}^2 \cdot f_{0\rightarrow1} \\
= C_L V_{DD}^2 \cdot f \cdot P_{0\rightarrow1} \\
= C_{switched} V_{DD}^2 \cdot f
\]

- Power dissipation is data dependent – depends on the switching probability
- Switched capacitance \( C_{switched} = C_L \cdot P_{0\rightarrow1} \)

**Transition Activity and Power**

- Energy consumed in \( N \) cycles, \( E_N \):

\[
E_N = C_L \cdot V_{DD}^2 \cdot n_{0\rightarrow1}
\]

\( n_{0\rightarrow1} \) – number of 0→1 transitions in \( N \) cycles

\[
P_{avg} = \lim_{N\rightarrow\infty} \frac{E_N}{N} \cdot f = \left( \lim_{N\rightarrow\infty} \frac{n_{0\rightarrow1}}{N} \right) \cdot C_L \cdot V_{DD}^2 \cdot f
\]

\[
\alpha_{0\rightarrow1} = \lim_{N\rightarrow\infty} \frac{n_{0\rightarrow1}}{N} \cdot f
\]

\[
P_{avg} = \alpha_{0\rightarrow1} \cdot C_L \cdot V_{DD}^2 \cdot f
\]
**Factors Affecting Transition Activity**

- "Static" component (does not account for timing)
  - Type of Logic Function (NOR vs. XOR)
  - Type of Logic Style (Static vs. Dynamic)
  - Signal Statistics
  - Inter-signal Correlations

- "Dynamic" or timing dependent component
  - Circuit Topology
  - Signal Statistics and Correlations

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**Type of Logic Function: NOR vs. XOR**

Example: Static 2-input NOR Gate

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
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<td>1</td>
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</tr>
</tbody>
</table>

Assume signal probabilities

\[ p_{A=1} = \frac{1}{2} \]
\[ p_{B=1} = \frac{1}{2} \]

Then transition probability

\[ p_{0\to1} = p_{\text{Out}=0} \times p_{\text{Out}=1} \]

\[ = \frac{3}{4} \times \frac{1}{4} = \frac{3}{16} \]

If inputs switch every cycle

\[ \alpha_{0\to1} = \frac{3}{16} \]
Type of Logic Function: NOR vs. XOR

Example: Static 2-input XOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
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<tbody>
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</tr>
</tbody>
</table>

Assume signal probabilities
- $p_{A=1} = 1/2$
- $p_{B=1} = 1/2$

Then transition probability

$$p_{0 \rightarrow 1} = p_{Out=0} \times p_{Out=1} = \frac{1}{2} \times \frac{1}{2} = \frac{1}{4}$$

If inputs switch in every cycle

$$\alpha_{0 \rightarrow 1} = \frac{1}{4}$$

Power Consumption of Dynamic Gates

Power only dissipated when previous Out = 0

In1  In2  In3  PDN

CLK  $M_p$

Out  $C_L$

CLK  $M_n$
Dynamic Power Consumption is
Data Dependent

Dynamic 2-input NOR Gate

Assume signal probabilities
\( P_{A=1} = 1/2 \)
\( P_{B=1} = 1/2 \)

Then transition probability
\( P_{0\rightarrow1} = P_{\text{out}=0} \times P_{\text{out}=1} \)

\[ = \frac{3}{4} \times 1 = \frac{3}{4} \]

Switching activity always higher in dynamic gates!

\( P_{0\rightarrow1} = P_{\text{out}=0} \)

Dynamic CVSL

Guaranteed transition for every operation!

\( \alpha_{0\rightarrow1} = 1 \)
**Problem: Reconvergent Fanout**

![Diagram of a reconvergent fanout circuit](image)

\[ P(Z = 1) = P(B = 1) \cdot P(X = 1 | B=1) \]

Becomes complex and intractable fast

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**Inter-Signal Correlations**

![Diagram of logic circuits](image)

Logic without reconvergent fanout

\[ p_{0\rightarrow1} = (1 - p_A p_B) \cdot p_A p_B \]

Logic with reconvergent fanout

\[ P(Z = 1) = p(C=1 | B=1) \cdot p(B=1) \]

\[ p_{0\rightarrow1} = 0 \]

- Need to use conditional probabilities to model inter-signal correlations
- CAD tools required for such analysis
**Glitching in Static CMOS**

The result is correct, but there is extra power dissipated.

*Also known as dynamic hazards*

**Example: Chain of NOR Gates**
Principles for Power Reduction

- Prime choice: Reduce voltage!
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question (0.6 … 0.9 V by 2010!)
  - Reducing thresholds to improve performance increases leakage
- Reduce switching activity
- Reduce physical capacitance

Sequential Logic
**Sequential Logic**

2 storage mechanisms
- positive feedback
- charge-based

**Latch versus Register**

- Latch stores data when clock is low
- Register stores data when clock rises
**Naming Convention**

- In our book, latch is level sensitive, register is edge-triggered.
- There are many different naming conventions.
- Many books call edge-triggered elements flip-flops.

**Latches**

Positive Latch

- **In** → **D** → **Q** → **Out**
- **clk**
- **In** → **Out** stable
- **Out follows In**

Negative Latch

- **In** → **D** → **Q** → **Out**
- **clk**
- **In** → **Out** stable
- **Out follows In**
**Latch-Based Design**

- N latch is transparent when $\phi = 0$
- P latch is transparent when $\phi = 1$

**Timing Definitions**

[Diagram showing timing definitions with labels for $t_{\text{rise}}$, $t_{\text{fall}}$, $t_{\text{setup}}$, and $t_{\text{hold}}$.]
Characterizing Timing

\[ D \rightarrow Q \quad t_C \rightarrow Q \]

Register

\[ D \rightarrow Q \quad t_D \rightarrow Q \]

Latch

Maximum Clock Frequency

\[ t_{clk-Q} + t_{p,comb} + t_{setup} = T \]

Also:
\[ t_{cdreg} + t_{calogic} > t_{hold} \]
\[ t_{ef}; contamination delay = minimum delay \]
**Positive Feedback: Bi-Stability**

$V_{o2} = V_{i1}$

$V_{o1} = V_{i2}$

**Meta-Stability**

Gain should be larger than 1 in the transition region
**Writing into a Static Latch**

Use the clock as a decoupling signal, that distinguishes between the transparent and opaque states.

Converting into a MUX

Forcing the state (can implement as NMOS-only)

**Pseudo-Static Latch**

D  
CLK  
D  
CLK  
D  
CLK  
D
**Mux-Based Latches**

Negative latch  
(transparent when CLK = 0)

Positive latch  
(transparent when CLK = 1)

\[
Q = \overline{\text{Clk}} \cdot Q + \text{Clk} \cdot \text{In}
\]

\[
Q = \text{Clk} \cdot Q + \overline{\text{Clk}} \cdot \text{In}
\]

**Mux-Based Latch**

- D
- CLK
- Q
**Mux-Based Latch**

NMOS only

Non-overlapping clocks

**Storage Mechanisms**

Static

Dynamic
Next Lecture

- Sequential logic (cntd)